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## A Novel Cascaded Multilevel Converter

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**A NOVEL CASCADED MULTILEVEL CONVERTER**

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Bachelor of Electrical Engineering

Anna University

May, 2005

Submitted in partial fulfillment of requirements for the degree

**MASTER OF SCIENCE IN ELECTRICAL ENGINEERING**

at the

**CLEVELAND STATE UNIVERSITY**

August, 2008

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## **DEDICATION**

I dedicate this thesis to my dad Rangarajan Ramanujam, mom Kalavathy Rangarajan, my beloved brother Hari Prashad Rangarajan and my friends Ravi and Charles.

I thank all my friends in this country and abroad for their love and care.

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I thank all my friends in this country and abroad for their love and care.

# **A NOVEL CASCADED MULTILEVEL CONVERTER**

**RAJMOHAN RANGARAJAN**

## **ABSTRACT**

A novel cascaded multilevel converter is proposed in this thesis. The thesis proposes to produce more voltage levels from fewer H-bridges in a cascaded multilevel converter. The converter uses fewer H-bridges and the proposed switching scheme renders more voltage level in the staircase waveform with equal steps. Since the resulting voltage levels are equal, the angles are determined for the complete elimination of more unwanted harmonics. The implementation of the switching scheme, in single and three-phase configurations were simulated with Ansoft Simplorer<sup>®</sup> and the frequency spectrum of the resulting waveform and its total harmonic distortion are shown to verify the results. The number of switches employed in the converter is halved. The impact of voltage magnitude variations on harmonic elimination is analyzed. Source and switch utilization is also evaluated.

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## NOMENCLATURE

- AC: Alternating current
- BJT: Bipolar junction transistor
- DC: Direct current
- DPF: Displacement power factor
- GTO: Gate turn-off thyristor
- IGBT: Insulated-gate bipolar transistor
- MLC: Multilevel converter
- PF: Power factor
- SDCS: Separate DC source
- THD: Total harmonic distortion

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## CHAPTER I

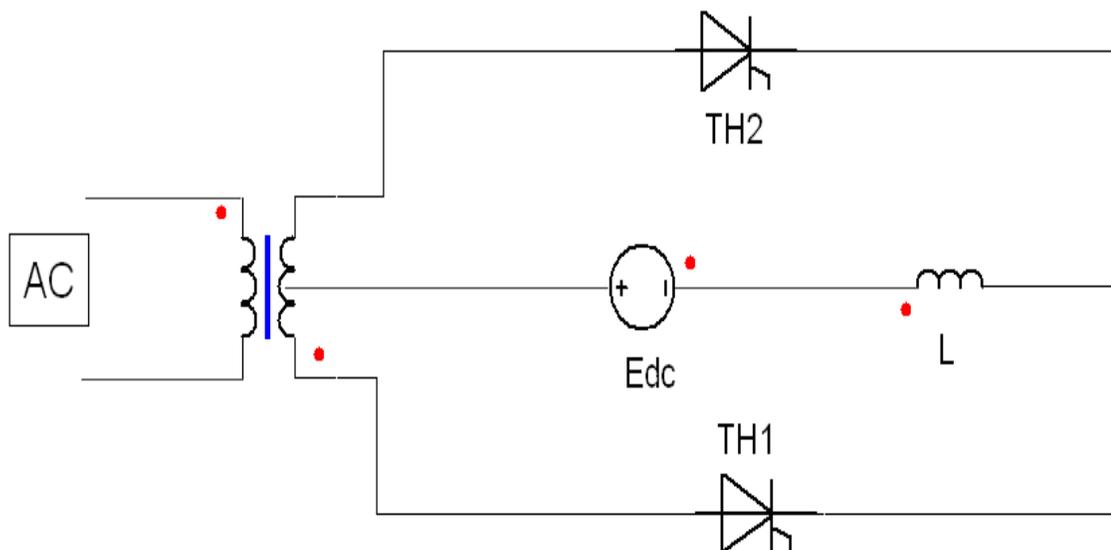
### INTRODUCTION

An inverter is a power electronic device that produces an alternating current (AC) from a direct current (DC) source. David Chandler Prince first reported the term *inverter* in a GE review ‘*The Inverter*’ [1]. According to Prince, the term *inverter* means any stationary or rotating apparatus that transforms alternating current to direct current.

Early AC to DC converters employed an AC motor to drive a DC generator for rectification and was commonly referred to as *mechanically rectified DC*. The same motor-generator set was made to work backwards and this combination, produced AC from DC. This combination was commonly referred to as *inverted converter*. These mechanized power converters were later replaced by solid-state converters, which employed vacuum tubes or gas filled tubes.

From the late nineteenth century to the middle twentieth century, vacuum tubes and gas-filled tubes were used as switches in the AC-DC and DC-AC converters. The thyatron was the most widely used device as the converter switch. In the year 1957, thyristors were introduced. The advent of thyristors was a breakthrough in solid-state switching devices.

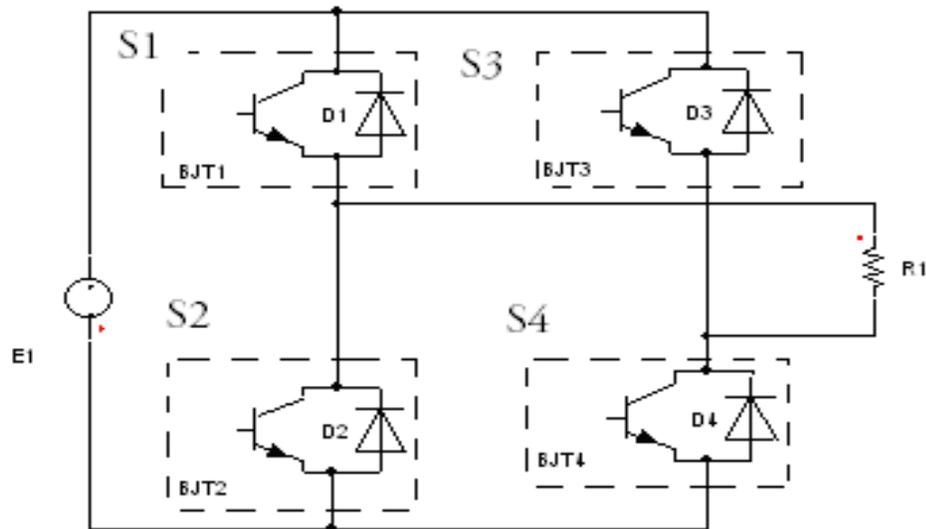
Many different topologies for single and three phase inverters were introduced. One of the early inverter topologies introduced by Prince is shown in Figure 1. The inverter was realized with two solid-state switches and a center-tapped transformer. The center-tapped side of the transformer is the input side. One terminal of the DC source is connected to the center-tapped terminal of the transformer. The other two terminals of the transformer are connected to the solid-state switches. The AC voltage appears across the output terminals of the inverter. The positive half of the AC voltage is obtained when switch TH1 is turned on and switch TH2 remains in the off-state. The other half of the AC voltage results when switch TH2 is turned on and switch TH1 is turned off. The inverter topology is also known as a half-bridge inverter. The other basic topology of an inverter is the full-bridge inverter and it is the basic building block of a cascaded multilevel converter (MLC) [2].



**Figure 1:** Prince's inverter

## 1.1 Full-bridge inverter

A full-bridge inverter consists of two half-bridge inverters. The corresponding circuit diagram is shown in Figure 2.

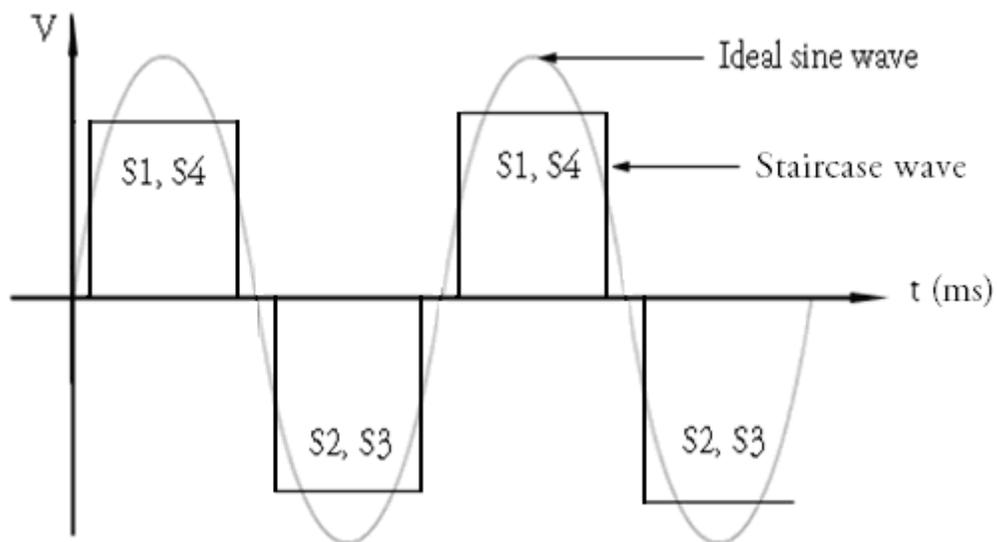


**Figure 2:** Single-phase full-bridge inverter

A single-phase full-bridge inverter is made up of four transistors and four diodes. The transistor can be replaced by other solid-state switches like thyristor, MOSFET, GTOs, and IGBTs etc. Solid-state switches are unidirectional switches i.e. they conduct in only one direction. A diode is connected anti-parallel to each transistor to realize a bidirectional switch. Due to the circuit's close resemblance to the letter 'H', the full-bridge inverter is also known as an *H-bridge* inverter.

The operation of the H-bridge inverter is as follows. The set BJT1 and D1 is switch S1, BJT2 and D2 is S2 and so on. To produce the positive half cycle of the waveform, switches S1 and S4 are turned on. The current flows from the positive

terminal of the DC source through switch S1, load, and switch S4 to the negative terminal of the battery. To produce the negative half cycle of the voltage waveform, switches S1 and S4 are turned off. Switches S2 and S3 are turned on, current flows from the positive terminal of the battery through switch S3, load, and switch S2, but the direction of the current is reversed to that in the previous case. Thus, an alternating staircase waveform is produced across the terminals of the AC load. The waveform is shown in Figure 3.



**Figure 3:** Staircase waveform from an H-bridge inverter

The switching table for the inverter is listed in Table I. In the switching table, one signifies on-state and zero signifies off-state.

**Table I:** Switching table for H-bridge inverter

Switch				Voltage
S1	S2	S3	S4	
1	0	1	0	0
1	0	0	1	+V
0	1	1	0	-V
0	1	0	1	0

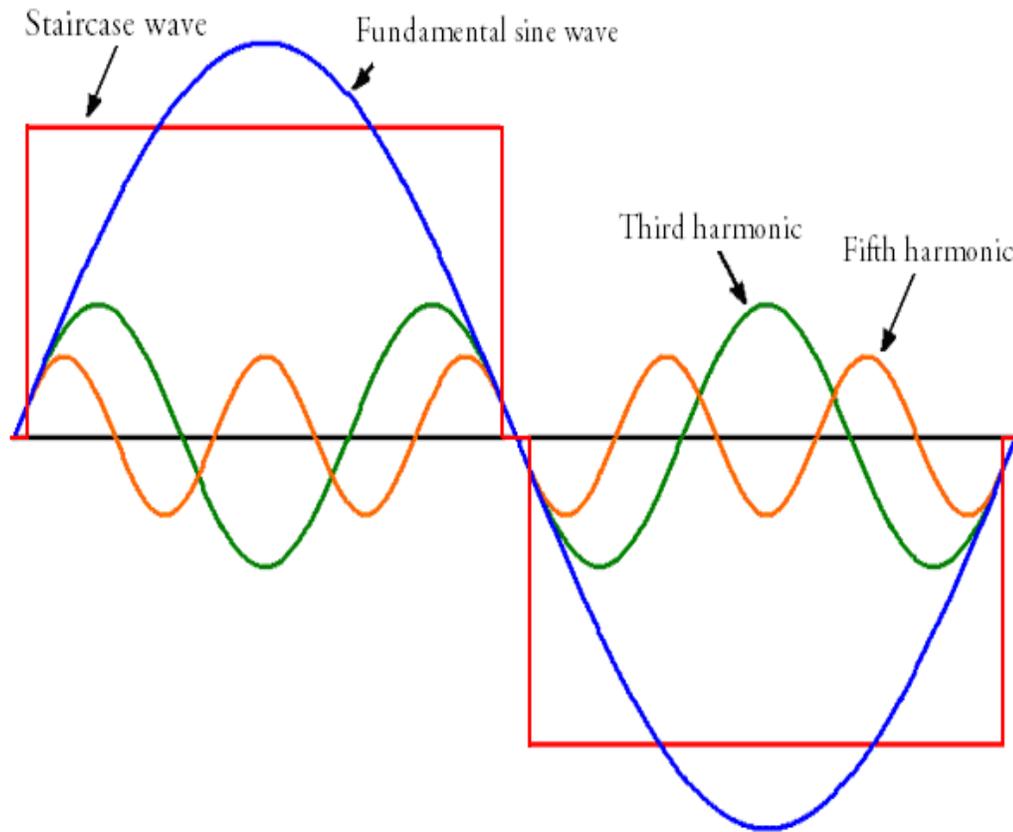
The output from the inverter is a periodically alternating staircase waveform, not a sinusoidal waveform as expected. The output waveform is far from an ideal sine waveform. The output waveform from the inverter contains harmonics.

## 1.2 Harmonics

Harmonics are undesired oscillations in a system and they oscillate at integer multiples of the fundamental frequency. The voltage and current waveform in an AC system should be sinusoidal with constant amplitude, constant and single frequency. The harmonics distort the waveform of the fundamental.

A staircase wave can be decomposed into its fundamental component and its harmonic components using Fourier series and is pictorially represented in Figure 4. In Figure 4, only the fundamental, the third and the fifth harmonics are shown for simplicity. Mathematically, the waveform is a summation of an infinite series of harmonics. The magnitude of the harmonics, decrease with increase in the harmonic

number. Harmonics must always be limited below threshold levels prescribed by standards [5], both in their THD and individual magnitudes.



**Figure 4:** A staircase wave decomposed into its fundamental and first few of its harmonics

The amount of distortion in the voltage or current waveform is quantified by means of an index called the total harmonic distortion (THD). The performance of a power-electronic device is dependent on the harmonic content in the output waveform. The THD in the voltage or current waveform is mathematically defined as the ratio of distortion current to the fundamental current. The formula to compute THD is given in equation 1.

$$\begin{aligned}
 THD &= \frac{|I_{dist}|}{|I_1|} \times 100 \\
 &= \sqrt{\left(\frac{|I|}{|I_1|}\right)^2 - 1} \times 100
 \end{aligned}
 \tag{1}$$

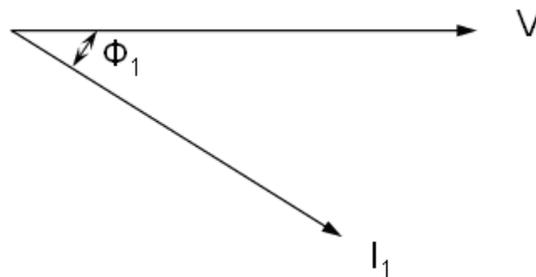
The THD of a system greatly affects the active power in the system. The apparent power in a system is the product of the rms values of the voltage and current and is given by equation 2.

$$S = |V_s| |I_s| \tag{2}$$

The real power in the system is the product of voltage, current and the cosine of the angle ( $\phi$ ) between the voltage and current and is expressed by equation 3.

$$P = |V_s| |I_s| \cos \phi \tag{3}$$

The cosine term in the above equation is defined as the power factor of the system. The phasor representation of the system voltage and the current (current lagging the voltage) is shown in Figure 5.



**Figure 5:** Phasor representation of voltage and current

Displacement power factor is defined as the cosine of the phase angle between the voltage and fundamental current. In a system without harmonics, the displacement power factor (dpf) is equal to the system power factor. Assuming a perfectly sinusoidal voltage, the power factor (pf) of the system is obtained as follows.

$$pf = \frac{|P|}{|S|} = \frac{|V_s| |I_{s,1}| \cos \phi_1}{|V_s| |I_s|}$$

$$pf = \frac{|I_{s,1}|}{|I_s|} \cos \phi_1$$

$$dpf = \cos \phi_1$$

$$pf = \frac{1}{\sqrt{1 + THD^2}} \cdot dpf \quad (4)$$

The harmonics present in the system thus decreases the power factor of the system.

Harmonics, being high frequency components of the fundamental, the harmonic voltages and currents flow through the periphery of the conductor and decrease the cross-sectional area of the conductor. This results in the increase in the equivalent resistance of the conductor. This induces overheating in the wiring of motors, transformers and other electrical devices. It results in premature breakdown of the insulating materials and the reduction in the lifetime of the electrical machines. Thus, harmonics reduce the reliability and efficiency of the system. In order to reduce or eliminate harmonics from the system, a thorough analysis of the harmonics present in the system is required. Fourier series is a very efficient tool to analyze any periodic function.

### 1.3 Periodic function

A function that repeats itself after a time-period  $T$  is defined as a periodic function. Mathematically a periodic function is defined in equation 5.

$$f(t) = f(t+T) \quad (5)$$

A periodic function is classified based on the functionality of the waveform and the symmetry of the waveform. Based on the functionality, a periodic function  $f(t)$  can be an even function, an odd function, or an arbitrary function. An even function is mathematically defined in equation 6 and an odd function is mathematically defined in equation 7.

$$f(t) = f(-t) \quad (6)$$

$$f(t) = -f(t) \quad (7)$$

An arbitrary function is neither odd nor even, and is mathematically represented in equation 8.

$$f(t) = f_{even}(t) + f_{odd}(t) \quad (8)$$

Based on the symmetry of the waveform, a waveform can exhibit half-wave symmetry, quarter-wave symmetry or hidden symmetry. A periodic function  $f(t)$  is half-wave symmetric if it satisfies the property expressed mathematically in equation 9.

$$f(t) = -f\left(t + \frac{T}{2}\right) \quad (9)$$

A periodic function that is both half-wave symmetric and is an even or an odd function exhibits quarter-wave symmetry. If the periodic function  $f(t)$  is shifted in time by a constant, then the periodic function exhibits a hidden symmetry.

A periodic wave from the inverter can be decomposed into a series of fundamental and harmonic terms using Fourier analysis.

#### 1.4 Fourier series analysis

A periodic signal  $f(t)$  of period  $T$  can be expanded into a trigonometric Fourier series of the form,

$$f(t) = \frac{1}{2}a_0 + \sum_{k=1}^{\infty} [a_k \cos(k\omega t) + b_k \sin(k\omega t)] \quad (10)$$

where,

$$a_0 = \frac{2}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} f(t) dt$$

$$a_k = \frac{2}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} f(t) \cos(k\omega t) dt$$

$$b_k = \frac{2}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} f(t) \sin(k\omega t) dt$$

$$\omega = \frac{2\pi}{T}$$

Equation 10 can also be written in the following form.

$$f(t) = A_0 + \sum_{k=1}^{\infty} A_k \cos(k\omega t + \theta_k) \quad (11)$$

where,

$$A_0 = \frac{a_0}{2}$$

$$A_k = \sqrt{a_k^2 + b_k^2}$$

$$\theta_k = \arctan\left(-\frac{b_k}{a_k}\right)$$

$A_0$  is the DC component of the wave;  $A_k$  is the magnitude of the  $k^{\text{th}}$  harmonic component and  $\theta_k$  is the angle of the  $k^{\text{th}}$  harmonic component. The knowledge of harmonics and Fourier analysis is important to analyze the performance of the inverter and to improve the power quality of the AC voltage. The summary of the waveform symmetry and their respective Fourier coefficients are listed in Table II.

**Table II:** Fourier table summary

<b>Waveform symmetry</b>	<b>Definition</b>	<b>Fourier coefficients</b>	<b>Fourier coefficients equal to zero</b>
Even	$f(-t)=f(t)$	$a_k$	$b_k$
Odd	$f(-t)=-f(t)$	$b_k$	$a_k$
Half-wave	$f(t)=-f(t+T/2)$	$a_{2k-1}, b_{2k-1}$	$a_{2k}, b_{2k}$
Even, Quarter - wave	$f(-t)=f(t)$ <i>and</i> $f(t)=-f(t+T/2)$	$a_{2k-1}$	$a_{2k}, b_k$
Odd, quarter - wave	$f(-t)=-f(t)$ <i>and</i> $f(t)=-f(t+T/2)$	$b_{2k-1}$	$b_{2k}, a_k$

This thesis focuses on the improvement in the performance of a cascaded multilevel converter. The thesis employs Fourier series analysis as one of the tools of analysis. The improvement in power quality is achieved by reducing the THD.

## 1.5 Multilevel converter

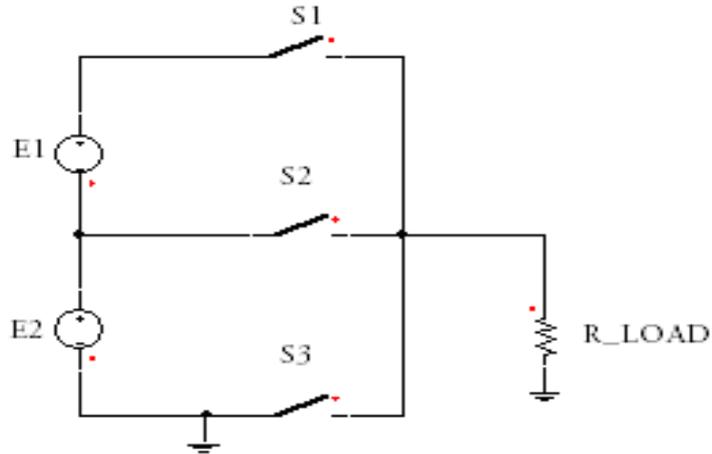
Multilevel converters emerged as a solution to produce a closer to sinusoidal output voltage and minimize the need for filtering. In addition, the multilevel converter operates at the fundamental switching frequency, which makes the multilevel converter suitable for high power applications [7]. Multilevel converters (MLC) commonly operate as inverters [2]. Multilevel converters include a string of semiconductor devices, fed by capacitor voltage sources or separate DC sources (SDCS) [8]. The term ‘level’ refers to the number of voltage steps ( $m$ ) produced by an MLC in one-quarter of a cycle (between zero and ninety degrees of an electric cycle). Typically the number of levels in a cascaded MLC is computed by  $m = (s+1)$ , where  $s$  is the number of DC sources. An MLC produces a staircase waveform from a single or multiple DC sources based on its topology.

The switching frequency in a multilevel converter is equal to the fundamental frequency (50 or 60 Hz). Hence, the loss due to frequency of switching is less. The switching losses in a solid-state device are proportional to the switching frequency and the number of switches in the system. The attractive features of multilevel converters are:

- a. Low switching  $dv/dt$*
- b. Low switching frequency*

The concept of multilevel voltage switching is as follows. Consider two DC sources connected as shown in Figure 6. The DC sources can be separate DC sources such as batteries. The magnitudes of the DC sources are equal. Three switches S1, S2 and S3 connect the DC sources to the load. The DC source switch combination is analogous

to a multilevel converter system, a multiple input DC system controlled by multiple switches to generate voltage potentials at various magnitudes.



**Figure 6:** Multilevel converter concept

When switch S3 is turned on with the other two switches in the off-state, the voltage across the load is zero. When switch S2 is turned on with switches S3 and S1 off, the voltage across the load is E2 and when S1 is on with switches S3 and S2 turned off, the voltage across the load is E1+E2. Thus a multi-potential environment is created in the system and the potential reflects across the load. The switching scheme that produces the voltage is summarized in table. In the table value zero for the switch signifies an off-state and value one signifies an on-state.

**Table III:** Multilevel voltage switching concept

Switch			Voltage across the load
S1	S2	S3	Volts
0	0	1	0
0	1	0	E1
1	0	0	E1+E2

There are three topologies of MLCs. They are,

- a. Diode clamped (neutral clamped) multilevel converter
- b. Flying capacitor (capacitor clamped) multilevel converter and
- c. Cascaded multilevel converter

The diode clamped and the flying capacitor type MLCs are fed from a single DC source. The DC voltage is equally divided employing a string of capacitors. In the diode clamped MLC, diodes are employed to clamp the voltages to produce a staircase voltage, hence the name *diode clamped* MLC. A diode clamped MLC is also known as *neutral-clamped* MLC. The voltage clamping to produce a staircase is achieved via capacitors in a flying capacitor type MLC. A flying-capacitor MLC is also known as *capacitor-clamped* MLC.

Due to the presence of a large number of capacitors in the flying capacitor MLC, the device is bulky and the operation and control of the device is complex. Hence, the diode clamped and cascaded MLC are the two topologies that are extensively employed for various applications.

The THD of the output voltage from a converter is limited by standards specifications. The THD of the output voltage can be reduced by eliminating or filtering out the harmonics from the system. The harmonics in the system can be filtered by passive low pass filters or the harmonics can be eliminated by harmonic elimination technique.

The harmonic elimination method involves solving complex trigonometric equations. The voltage magnitude of the DC sources impacts the elimination of

harmonics in the output voltage. Harmonic elimination is simple when the DC source voltage magnitudes are equal and constant. Several researches have been undertaken in the field of harmonic elimination.

A control strategy to maintain the capacitor voltages of a diode clamped MLC at a constant magnitude [10] was proposed. In this research the authors propose a mathematical model for a three-level diode clamped MLC and propose to control the uneven capacitor voltage magnitudes by an adaptive control technique. The control strategy is applicable only to the proposed mathematical model of the converter.

A method to solve the trigonometric equations for harmonic elimination using resultant theory [11] was proposed. In this research, resultant theory is employed as a method to simplify the trigonometric equations and obtain solutions for the equations. The work was extended and employed to eliminate harmonics in cascaded MLC with non-equal DC sources and the work was reported [12].

An active harmonic elimination technique, in which an FPGA processor is employed to measure and compute the firing angles for the elimination of harmonics in a cascaded MLC, was proposed [13]. The processor is coded to compute the firing angles for harmonic elimination in real time using resultant theory in real time and the results were published [13]. Several other researches that involve hybrid topologies for MLC, control strategies were reported, diode clamped and cascaded MLC being the focus.

This thesis proposes a novel cascaded multilevel converter which produces more voltage levels from the same number of H-bridges. The proposed cascaded multilevel converter does not modify the topology of the classical cascaded multilevel converter. The THD of the proposed converter is lesser than the classical converter.

Simulations performed to verify the functionality of the proposed switching scheme are furnished. The simulation was performed using Ansoft's Simplorer<sup>®</sup> program. The results of the simulation show the harmonic content in the simulated output and the THD of the system.

## **1.6 Organization of the thesis**

This thesis is organized as follows. Chapter II is an overview of cascaded multilevel converter. The chapter explains the theory of the converter, construction and operation. The decomposition of the produced periodic waveform from the multilevel converter into its Fourier components is shown. The section discusses harmonic elimination technique

Chapter III discusses the modified switching scheme for the multilevel converter. The supporting mathematical concepts are discussed. The chapter discusses both the integer multiple voltage magnitude case as well as the unequal voltage magnitude case. The concept of resultant theory and its application to find solutions for the Fourier transcendental equation is discussed.

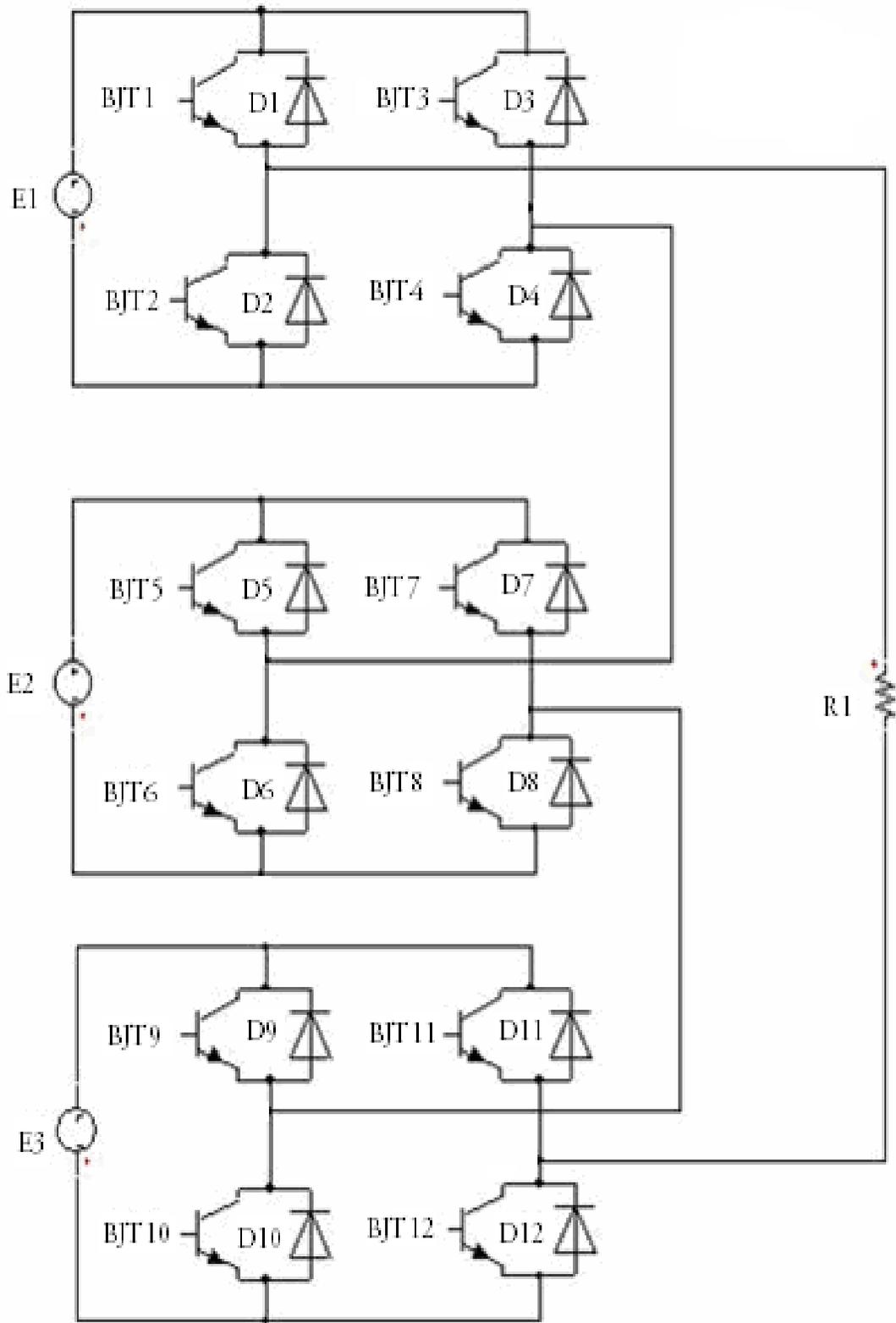
Chapter IV deals with the development of the simulation model. The simulated results are compared and the performance of the system is analyzed. The chapter also discusses the voltage sensitivity and its impact in harmonic elimination of the produced voltage.

Chapter V summarizes and concludes the work and is the prolegomenon to the future research areas in this technology.

## **CHAPTER II**

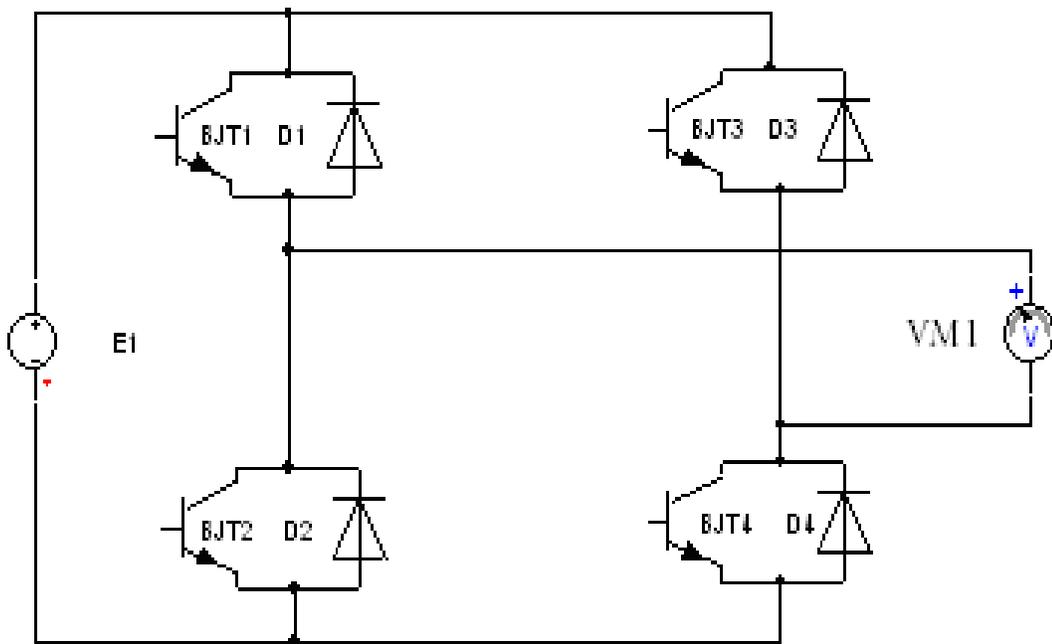
### **CASCADED MULTILEVEL CONVERTER**

A cascaded multilevel converter is realized by the series (cascaded) connection of H-bridge inverters. The functional building block of a cascaded multilevel converter is an H-bridge inverter. Each H-bridge in the converter is fed by an independent DC-source. An  $m$ -level cascaded MLC is made of  $m-1$  H-bridges and fed by  $m-1$  separate DC sources. The DC source can be batteries, solar arrays etc. The magnitudes of the independent DC sources are all equal. The rating of all the transistors and the diodes used in the switches are the same. A four-level, single-phase MLC is shown in Figure 7. The load is connected across the cascaded bridges as shown. All H-bridges are connected in series as shown in the Figure 7.



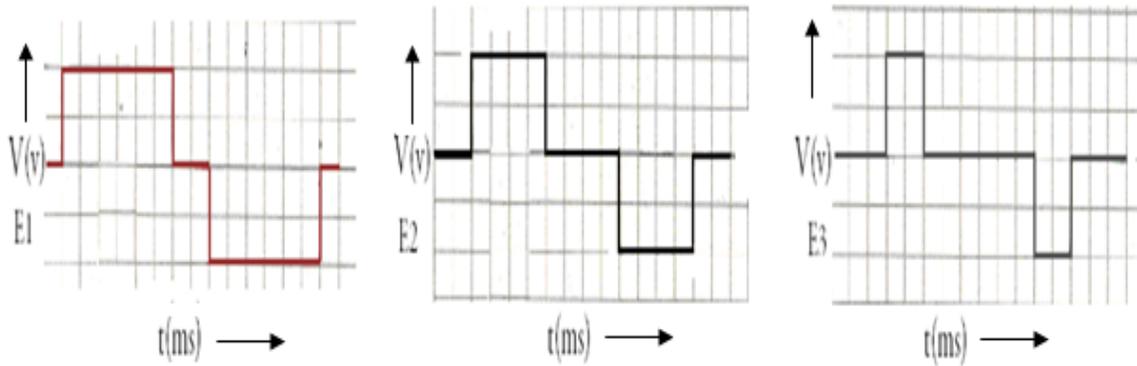
**Figure 7:** Four-level cascaded MLC

Like all the other topologies of the multilevel inverter, the cascaded multilevel inverter produces a staircase voltage across its output terminals. The step size in the output voltage is equal. The operation of the cascaded MLC is as follows. Each H-bridge in the cascaded MLC can produce a periodic staircase wave, independent of one another. These periodic staircase waves add up since the bridges are connected in series, producing a staircase voltage of equal step sizes. Consider an H-bridge cell of the cascaded MLC supplied by the DC source  $E_1$  in Figure 8.



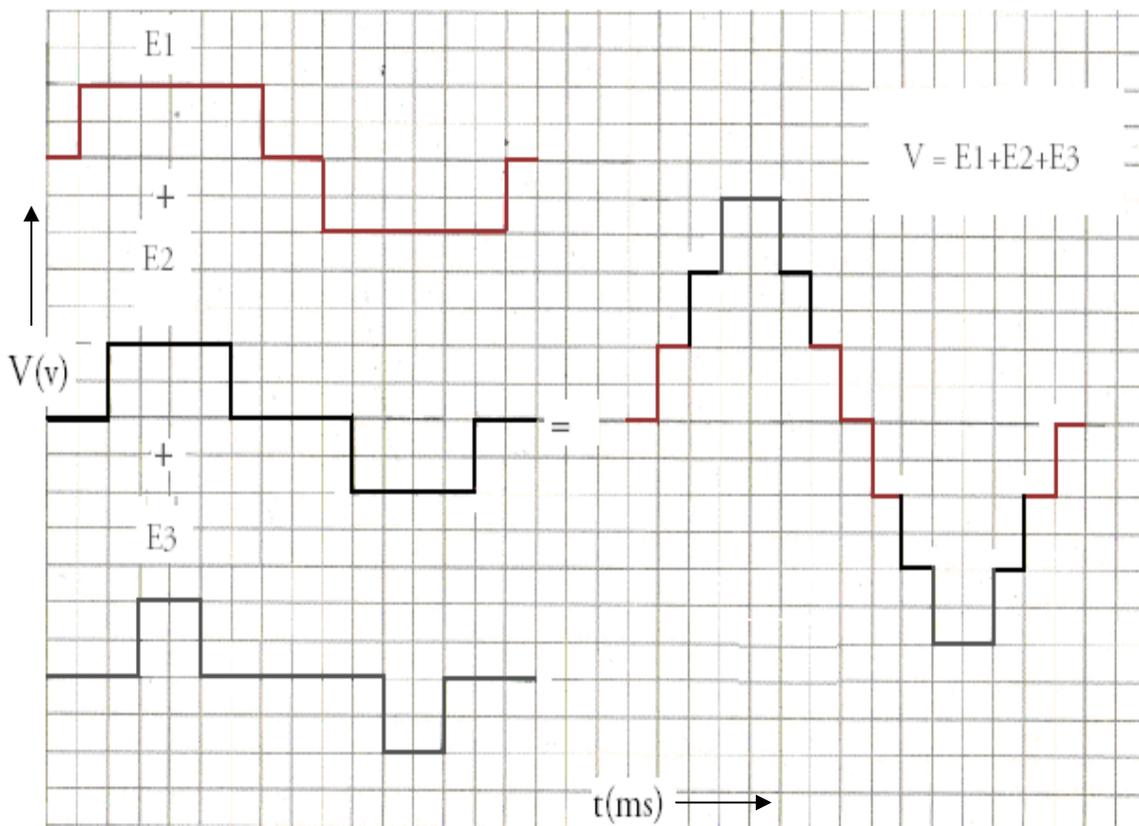
**Figure 8:** H-bridge cell

Switches BJT1 and BJT4 are turned on and switches BJT2 and BJT3 are turned off to produce the positive voltage. Switches BJT2 and BJT3 are turned on while BJT1 and BJT4 are turned off to produce the negative voltage. A similar switching scheme is employed in the other two H-bridges of the cascaded MLC. Similarly, the output voltage from each H-bridge is shown in Figure 9.



**Figure 9:** Produced output voltage from each H-bridge

The summation of the periodic output voltages from each H-bridge inverter results in the required step voltage. The cascade connection of the H-bridge inverters results in the required staircase voltage. This is shown in Figure 10<sup>†</sup>.

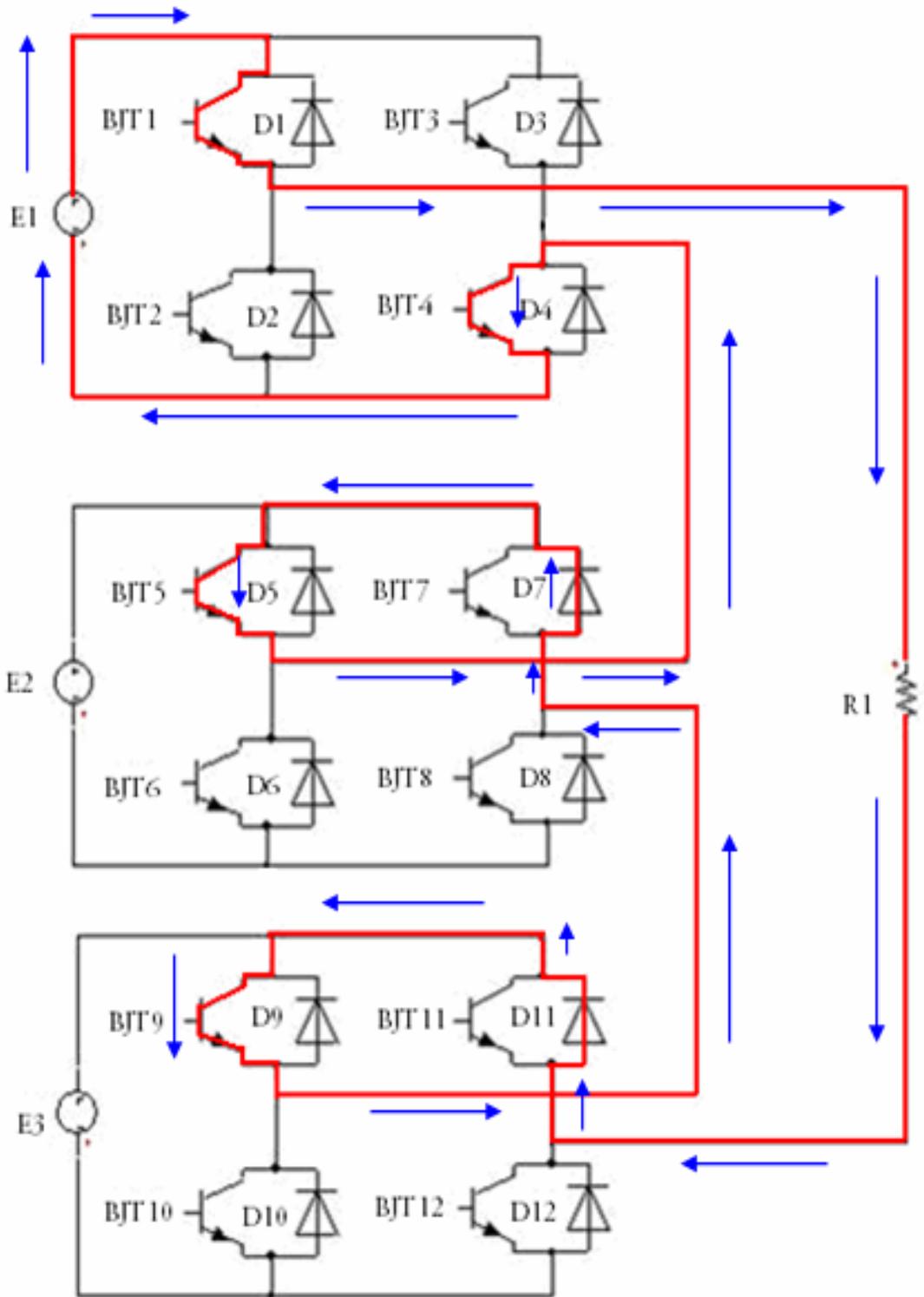


**Figure 10:** Output voltage based on the classical switching scheme

<sup>†</sup> - Graph not drawn to scale

The H-bridge inverter fed by the sources E2 and E3 remains turned off for a finite time after the H-bridge fed by source E1 is turned on. During this delay there is no flow of current in through the switches and hence, no voltage appears across the output terminals of the multilevel converter. This difficulty is overcome by turning on the switches connected to the same source terminals. While synthesizing the positive half of the cycle, the BJTs connected to the positive terminals of the non-synthesizing H-bridge are turned on.

For example, to produce a 100 V across the source, BJT1 and BJT4 are turned on. In the other two non-synthesizing H-bridges, BJT5, BJT7, BJT9 and BJT11 are turned on. The BJT5 and BJT9 conduct naturally. The BJT7 and BJT11 cannot conduct current in the opposite direction as they are uni-directional switches. BJT7 and BJT11 receive positive gate pulses and the voltage across the collector emitter junction is zero which short-circuits the diodes D7 and D11 respectively, thus providing a closed path for the flow of current for all voltage levels, at all times. The scheme is pictorially represented in Figure 11.



**Figure 11:** Current path illustration for 100 V case

The switching table for all the voltage levels and the switch combinations are listed in Table IV. In the switching table, one signifies an on-state and zero signifies an off-state.

**Table IV:** Switching table for MLC

Voltage (V)	BJT 1	BJT 2	BJT 3	BJT 4	BJT 5	BJT 6	BJT 7	BJT 8	BJT 9	BJT 10	BJT 11	BJT 12
100	1	0	0	1	1	0	1	0	1	0	1	0
200	1	0	0	1	1	0	0	1	1	0	1	0
300	1	0	0	1	1	0	0	1	1	0	0	1
0	1	0	1	0	1	0	1	0	1	0	1	0
-100	0	1	1	0	0	1	0	1	0	1	0	1
-200	0	1	1	0	0	1	1	0	0	1	0	1
-300	0	1	1	0	0	1	1	0	0	1	1	0

To summarize, an  $m$ -level cascaded multilevel inverter consists of  $m-1$  number of H-bridges,  $m-1$  number of separate DC sources and  $4(m-1)$  numbers of switches.

The H-bridge inverter fed by DC source E3 conducts for shorter durations than the inverter fed by source E2 which in turn has a less conduction time than the inverter fed by source E1.

The discharge rate of the DC sources is not equal in an electric-cycle. This difficulty is overcome by sequencing the H-bridges every cycle to even out the battery discharge rates.

## 2.1 Sequencing

Sequencing is a method in which the conduction time of a DC source is varied. In a cascaded MLC, the conduction time of the DC sources are unequal. One DC source is discharged for a longer time-period than the other DC source. By sequencing the switching pattern is varied such that the discharge rate of the DC-sources is evened out over a period of time. The concept of sequencing is explained as follows.

Consider two separate DC sources ( $A$ ,  $B$ ) of equal voltage magnitudes. Let the discharge of  $A$  be twice of that of  $B$ .

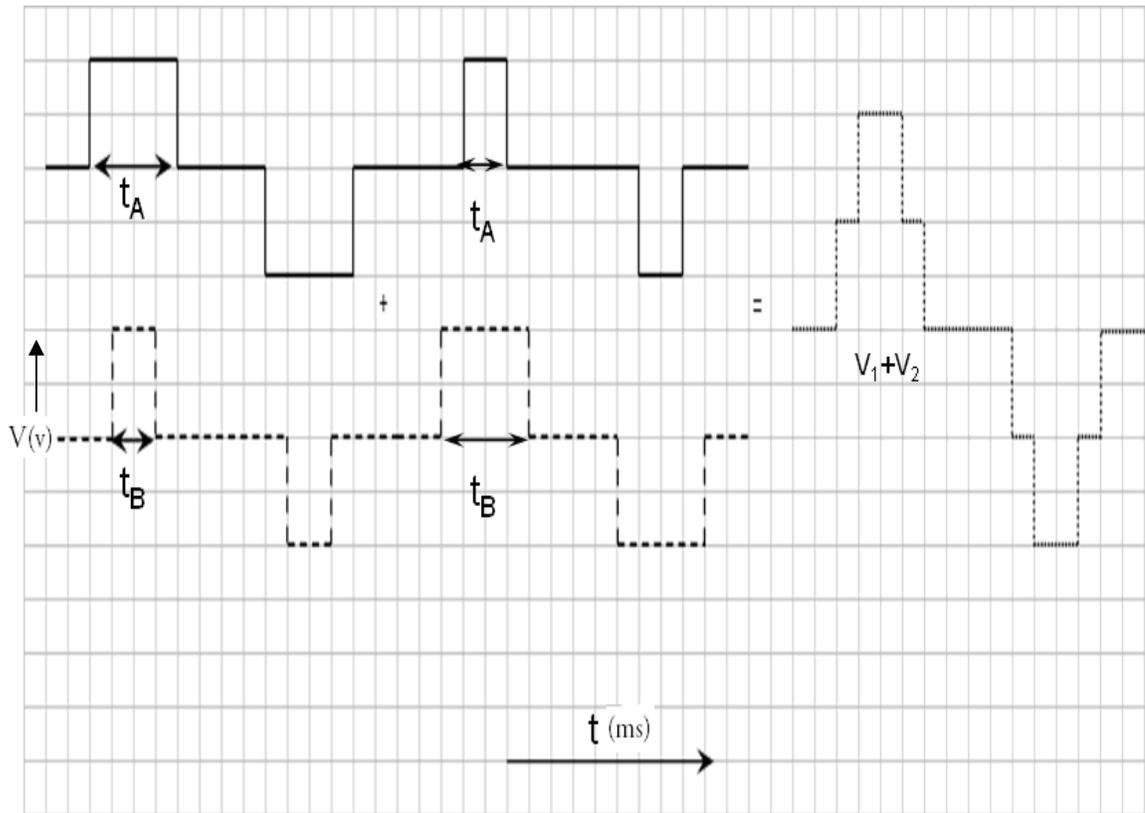
$$t_A = 2t_B$$

The voltage magnitudes of the two sources are equal. Hence in the second cycle the switching of the semi-conductors are varied such that the discharge rate of  $B$  is twice that of  $A$ .

$$t_B = 2t_A$$

Thus the discharge rates of the DC sources are even out every two cycles by sequencing. Sequencing is pictorially shown in Figure 12<sup>†</sup>. Similarly sequencing can be carried out in an m-level cascaded multilevel converter to obtain an equal DC voltage source discharge rate.

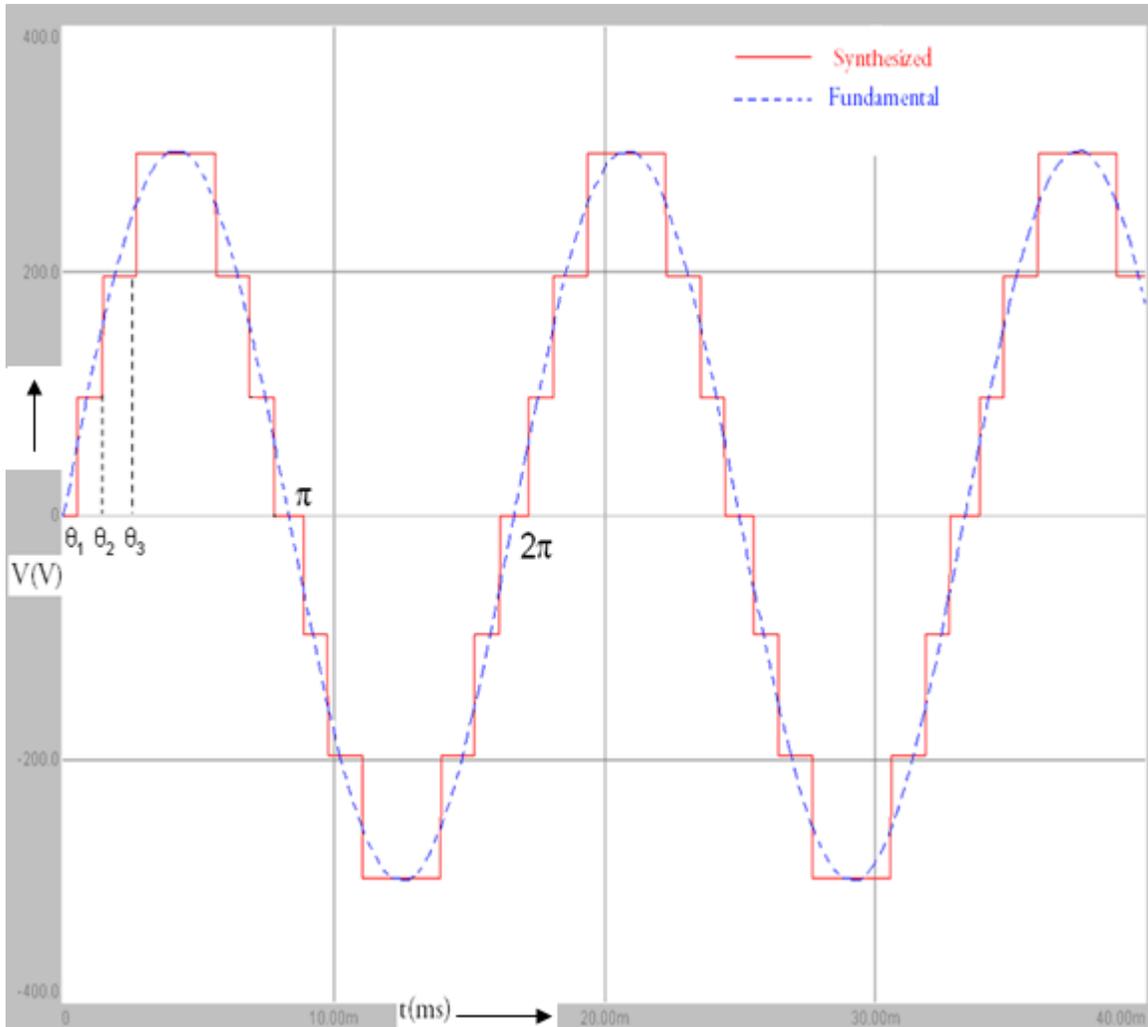
† - Graph is not drawn to scale.



**Figure 12: Sequencing**

## 2.2 Fourier analysis of output waveform

The output voltage from the cascaded multilevel converter is decomposed into its Fourier components to analyze the harmonics present in the voltage, their respective magnitudes. This information quantifies to provide information on the THD of the output voltage from the cascaded MLC. The output obtained from a four-level cascaded MLC is analyzed using Fourier series. The simulated voltage is shown in Figure 13.



**Figure 13:** Four-level output waveform and its decomposed fundamental wave

The first step rise occurs at  $\theta_1$  and the subsequent rises occur at  $\theta_2$  and  $\theta_3$  respectively as shown in Figure 13. The step falls, by symmetry occur at  $\pi - \theta_1$ ,  $\pi - \theta_2$ , and  $\pi - \theta_3$  respectively.

The analysis of the voltage function based on its periodicity is as follows.

1. The function repeats itself after a time period T, hence the function is periodic

2. The function satisfies the condition,  $f(-t) = -f(t)$ . Hence the function is an odd function.
3. The function satisfies the property,  $f(t) = -f(t+T/2)$ . Hence the function is half-wave symmetric.
4. The function exhibits odd symmetry and half-wave symmetry. Hence the function is an odd, quarter-wave, symmetric function.

A general case for the voltage steps is assumed. From the Fourier table summary (Table II12), the Fourier coefficients present in the given voltage function will be the  $b_{2k-1}$  terms, where  $k = 1, 3, 5 \dots \infty$ .

$$b_{2k-1} = \frac{4}{\pi} \int_0^{\frac{\pi}{2}} v(t) \sin(k\omega t) d\omega t \quad (12)$$

Substituting the function of the waveform in equation 12,

$$b_{2k-1} = \frac{4}{\pi} \left( \int_{\theta_1}^{\frac{\pi}{2}} V_1 \sin(k\omega t) d\omega t + \int_{\theta_2}^{\frac{\pi}{2}} V_2 \sin(k\omega t) d\omega t + \int_{\theta_3}^{\frac{\pi}{2}} V_3 \sin(k\omega t) d\omega t \right) \quad (13)$$

Integrating equation 13,

$$b_{2k-1} = -\frac{4}{\pi} \left( [V_1 \cos(k\omega t)]_{\theta_1}^{\frac{\pi}{2}} + [V_2 \cos(k\omega t)]_{\theta_2}^{\frac{\pi}{2}} + [V_3 \cos(k\omega t)]_{\theta_3}^{\frac{\pi}{2}} \right) \quad (14)$$

We know that,

$$\cos\left(\frac{k\pi}{2}\right) = 0$$

Substituting the lower and upper limits in equation 14,

$$b_{2k-1} = \frac{4}{\pi} (V_1 \cos(k\theta_1) + V_2 \cos(k\theta_2) + V_3 \cos(k\theta_3)) \quad (15)$$

Substituting the Fourier coefficient we get the Fourier series of the given voltage function is as follows.

$$v(t) = \frac{4}{\pi} \sum_k (V_1 \cos(k\theta_1) + V_2 \cos(k\theta_2) + V_3 \cos(k\theta_3)) \sin(k\omega t) \quad (16)$$
$$k = 1, 3, 5 \dots \infty$$

Under ideal conditions, the voltage magnitudes of each step are assumed equal, i.e.  $V_1 = V_2 = V_3 = V_{DC}$ .

The harmonics lead to poor performance of electrical systems and deteriorate the life of electrical and electronic devices. The THD of the produced voltage is high and does not meet the standards specifications. The need for elimination of as many harmonics out of the system as possible becomes a priority. The harmonics can either be filtered out of the system by using a low pass filter or by employing harmonic elimination technique [9]. Filtering techniques need passive, low-pass filters. The elimination of harmonics without the need for filters is an economic choice.

### 2.3 Harmonic elimination technique

Harmonic elimination technique is a method to get rid of harmonics by judicious selection of the firing angles of the inverter. The harmonics elimination technique eliminates the need for expensive low pass filters in the system. The harmonic elimination begins with the Fourier series of the produced voltage. From equation 16, the fundamental voltage of the produced output is given by,

$$v_1(t) = \frac{4}{\pi} (V_1 \cos(\theta_1) + V_2 \cos(\theta_2) + V_3 \cos(\theta_3)) \sin(\omega t) \quad (17)$$

The third, fifth and the seventh harmonic of the system are given by the following set of equations.

$$v_3(t) = \frac{4}{\pi} (V_1 \cos(3\theta_1) + V_2 \cos(3\theta_2) + V_3 \cos(3\theta_3)) \sin(3\omega t) \quad (18)$$

$$v_5(t) = \frac{4}{\pi} (V_1 \cos(5\theta_1) + V_2 \cos(5\theta_2) + V_3 \cos(5\theta_3)) \sin(5\omega t) \quad (19)$$

$$v_7(t) = \frac{4}{\pi} (V_1 \cos(7\theta_1) + V_2 \cos(7\theta_2) + V_3 \cos(7\theta_3)) \sin(7\omega t) \quad (20)$$

Two different cases for the harmonic elimination technique are analyzed. The one in which step sizes in the staircase function are equal and the one in which the step sizes are unequal are considered.

### 2.3.1 Case I

In this case the voltage steps in the output voltage are assumed to be equal. When the cascaded MLC is fed by a battery source the magnitude of the DC voltage are equal, but when it is fed by a capacitor based source like a solar array, the magnitudes are not exactly equal. Hence an equal voltage magnitude case is the ideal condition of operation of an MLC. When the voltage steps are equal, the set of transcendental equations are as follows.

We know that,

$$V_1 = V_2 = V_3 = V_{dc}$$

$$\begin{aligned} v_1(t) &= \frac{4V_{dc}}{\pi} (\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3)) \sin(\omega t) \\ v_3(t) &= \frac{4V_{dc}}{\pi} (\cos(3\theta_1) + \cos(3\theta_2) + \cos(3\theta_3)) \sin(3\omega t) \\ v_5(t) &= \frac{4V_{dc}}{\pi} (\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3)) \sin(5\omega t) \\ v_7(t) &= \frac{4V_{dc}}{\pi} (\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3)) \sin(7\omega t) \end{aligned} \quad (21)$$

In a three phase system, the triplen harmonics cancel out each other. The phenomenon is mathematically proven as follows. Consider the third harmonic of the produced output.

$$v_{a3}(t) = \frac{4V_{dc}}{\pi} (\cos(3\theta_1) + \cos(3\theta_2) + \cos(3\theta_3)) \sin(3\omega t)$$

The voltages in the other two phases are shifted by 120 degrees each, and the equation is given as follows.

$$\begin{aligned}
v_{b3}(t) &= \frac{4V_{dc}}{\pi} \left( \begin{array}{c} \cos(3(\theta_1 + 120^\circ)) + \\ \cos(3(\theta_2 + 120^\circ)) + \\ \cos(3(\theta_3 + 120^\circ)) \end{array} \right) \sin(3\omega t) \\
&= \frac{4V_{dc}}{\pi} (\cos(3\theta_1) + \cos(3\theta_2) + \cos(3\theta_3)) \sin(3\omega t)
\end{aligned}$$

and

$$\begin{aligned}
v_{c3}(t) &= \frac{4V_{dc}}{\pi} \left( \begin{array}{c} \cos(3(\theta_1 + 240^\circ)) + \\ \cos(3(\theta_2 + 240^\circ)) + \\ \cos(3(\theta_3 + 240^\circ)) \end{array} \right) \sin(3\omega t) \\
&= \frac{4V_{dc}}{\pi} (\cos(3\theta_1) + \cos(3\theta_2) + \cos(3\theta_3)) \sin(3\omega t)
\end{aligned}$$

Hence,

$$v_{a3}(t) = v_{b3}(t) = v_{c3}(t)$$

In a three-phase system,

$$v_{ab3}(t) = v_{a3}(t) - v_{b3}(t) = 0$$

Similarly,

$$v_{bc3}(t) = v_{ca3}(t) = 0 \tag{22}$$

Similarly, the other triplen harmonics cancel out each other. Hence, in a three phase system, one has to deal only with the other odd number harmonics. The amplitudes of the harmonics present in the output of the voltage are as follows.

$$\hat{V}_1 = \frac{4V_{dc}}{\pi} (\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3))$$

$$\hat{V}_5 = \frac{4V_{dc}}{\pi} (\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3))$$

$$\hat{V}_7 = \frac{4V_{dc}}{\pi} (\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3))$$

The fifth and seventh harmonic voltages are to be eliminated from the system. The number of harmonics that can be eliminated from the system depends on the number of levels in the output voltage of the MLC. In an m-level converter, m-2 number of harmonics can be eliminated. Therefore, in the four-level converter in this discussion, two harmonics can be eliminated. The equations are written as follows.

$$(\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3))\sin(\omega t) = \frac{\hat{V}_1\pi}{4V_{dc}}$$

$\hat{V}_1$  is the desired peak value of the fundamental voltage.

$$(\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3))\sin(5\omega t) = 0$$

$$(\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3))\sin(7\omega t) = 0 \quad (23)$$

By solving the above transcendental equations, the fifth and the seventh harmonic voltages can be eliminated from the system. The more the number of levels in the system, the more harmonics eliminated from the system.

### 2.3.2 Case II

In this case, the unequal step voltage size in the staircase voltage is considered. From equations (17) to (20), the amplitudes of the fundamental and the harmonics of the output voltage is given.

$$\hat{V}_1 = \frac{4}{\pi} (V_{1,dc} \cos(\theta_1) + V_{2,dc} \cos(\theta_2) + V_{3,dc} \cos(\theta_3))$$

$$\hat{V}_5 = \frac{4}{\pi} (V_{1,dc} \cos(5\theta_1) + V_{2,dc} \cos(5\theta_2) + V_{3,dc} \cos(5\theta_3))$$

$$\hat{V}_7 = \frac{4}{\pi} (V_{1,dc} \cos(7\theta_1) + V_{2,dc} \cos(7\theta_2) + V_{3,dc} \cos(7\theta_3))$$

The equations are rewritten to eliminate the harmonics from the system as follows.

$$\begin{aligned} (V_{1,dc} \cos(\theta_1) + V_{2,dc} \cos(\theta_2) + V_{3,dc} \cos(\theta_3)) &= \frac{\hat{V}_1 \pi}{4} \\ (V_{1,dc} \cos(5\theta_1) + V_{2,dc} \cos(5\theta_2) + V_{3,dc} \cos(5\theta_3)) &= 0 \\ (V_{1,dc} \cos(7\theta_1) + V_{2,dc} \cos(7\theta_2) + V_{3,dc} \cos(7\theta_3)) &= 0 \end{aligned} \quad (24)$$

Note:

$\hat{V}_1$  is the peak of the output voltage.

The set of transcendental equations in case II are more complex than the equations in case I. The solution for the transcendental equations is difficult to obtain even with the computational power available today.

To summarize, an  $m$ -level cascaded MLC requires  $(m-1)$  number of H-bridges,  $(m-1)$  number of SDCS and  $(m-2)$  number of harmonics can be eliminated from the output voltage.

### **CHAPTER III**

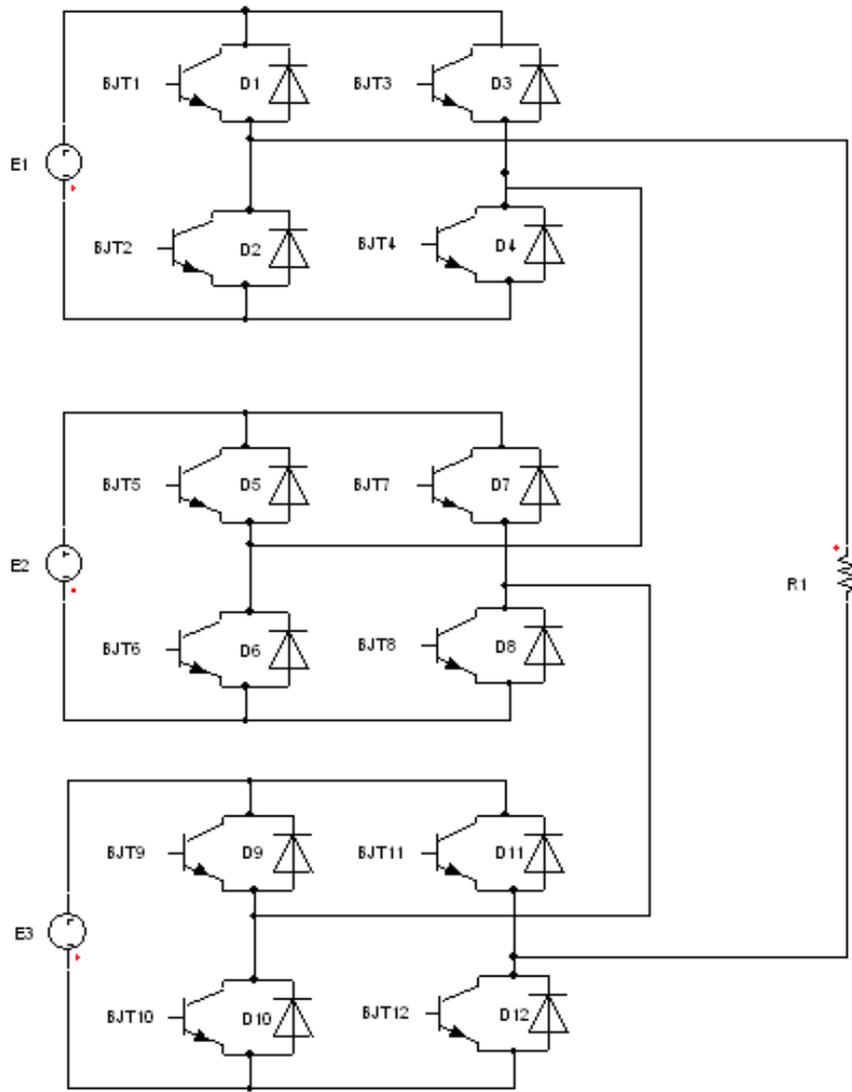
#### **PROPOSED CASADED MLC**

A cascaded multilevel converter fed by unequal DC sources is proposed and considered in this section. The magnitudes of the SDCS that feed the H-bridges are not equal but integer multiples of one another, i.e. an arithmetic progression. The switching of the inverter based on the previously developed switching scheme will produce a staircase waveform with unequal voltage steps at the output terminals.

A switching scheme is proposed to accommodate integer multiple magnitude voltage sources and to produce a staircase with equal step sizes. It will also be shown that the number of voltage levels of the staircase voltage waveform is increased for the same number of H-bridges and sources. Also, as a result of more levels, the THD in the resulting waveform is reduced since more harmonics can be eliminated.

### 3.1 Modified switching scheme

The modified switching scheme can be best explained by an example. Consider a cascaded MLC supplied by unequal but integer multiple sources. Let their magnitudes be 100 V, 200 V and 300 V respectively. The voltage sources are connected to three separate cascaded H-bridges as shown in Figure 14.



**Figure 14:** A four-level MLC fed by unequal DC sources

The classical switching scheme can produce a four level output. The first step in the voltage is zero volts, the second step is 100 V, the third step is 300 V and the fourth is 600 V.

In the modified switching scheme, the H-bridges are turned on and off to produce a 100 V step at each step of the produced staircase voltage. The magnitudes of the SDCS are an arithmetic progression. The voltage source in the system with the smallest magnitude is the 100 V source. The voltages in the output of the MLC can be made equal at steps in the following way.

When the H-bridge fed by source E3 is turned on, the voltage across the output will be 100 V. The semi-conductor switches in the other H-bridges are fired to provide a closed path for the flow of current from this bridge. In the next time instant the bridge is turned off and the bridge supplied by the source E2 is turned on. The semiconductor switches are turned on to provide a closed loop path. A 300 V step is produced by turning off the H-bridges supplied by sources E3 and E2, and turning on the H-bridge supplied by the source E1. To produce a 400 V step, H-bridges supplied by source E1 and E3 are turned on, while keeping the H-bridge supplied by the source E2 turned off. Likewise, a 500 V step is produced by turning on the H-bridges supplied with sources E2 and E1 while keeping the H-bridge with source E3 off. Finally, to produce the 600 V steps, all the H-bridges are turned on. The current path for a 400 V case is shown in Figure 15.

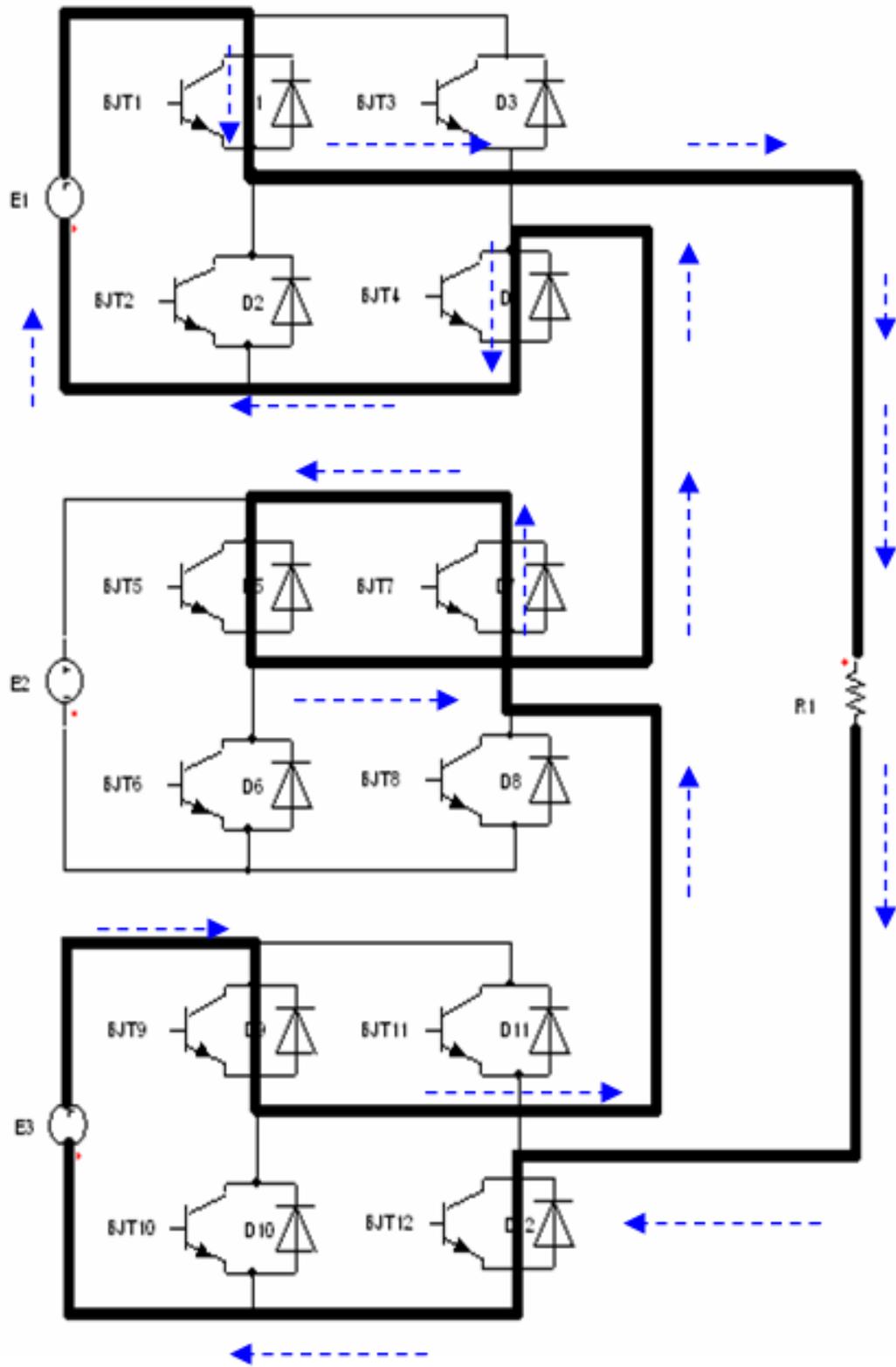
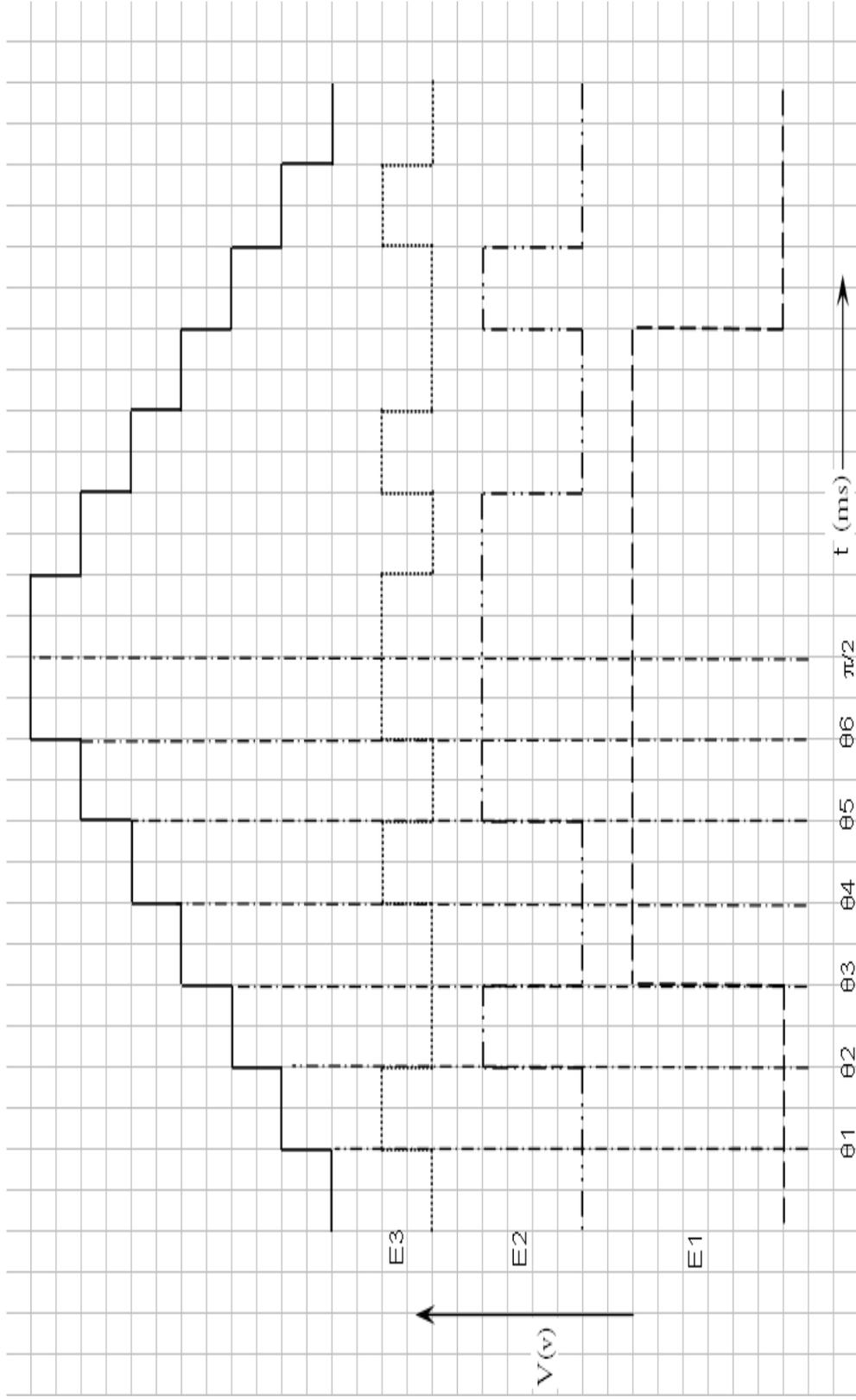


Figure 15: Current path to produce 400 V

The same logic is employed for the rest of the cycle and for every subsequent cycle. Thus, equal voltage steps are produced from the cascaded MLC fed by unequal SDCS. The synthesis of the staircase voltage is graphically shown in Figure 16. In Figure 16, the voltage synthesis for half cycle is shown. The firing angle  $\theta$  for the voltage steps are obtained by solving the Fourier equations for harmonic elimination technique.



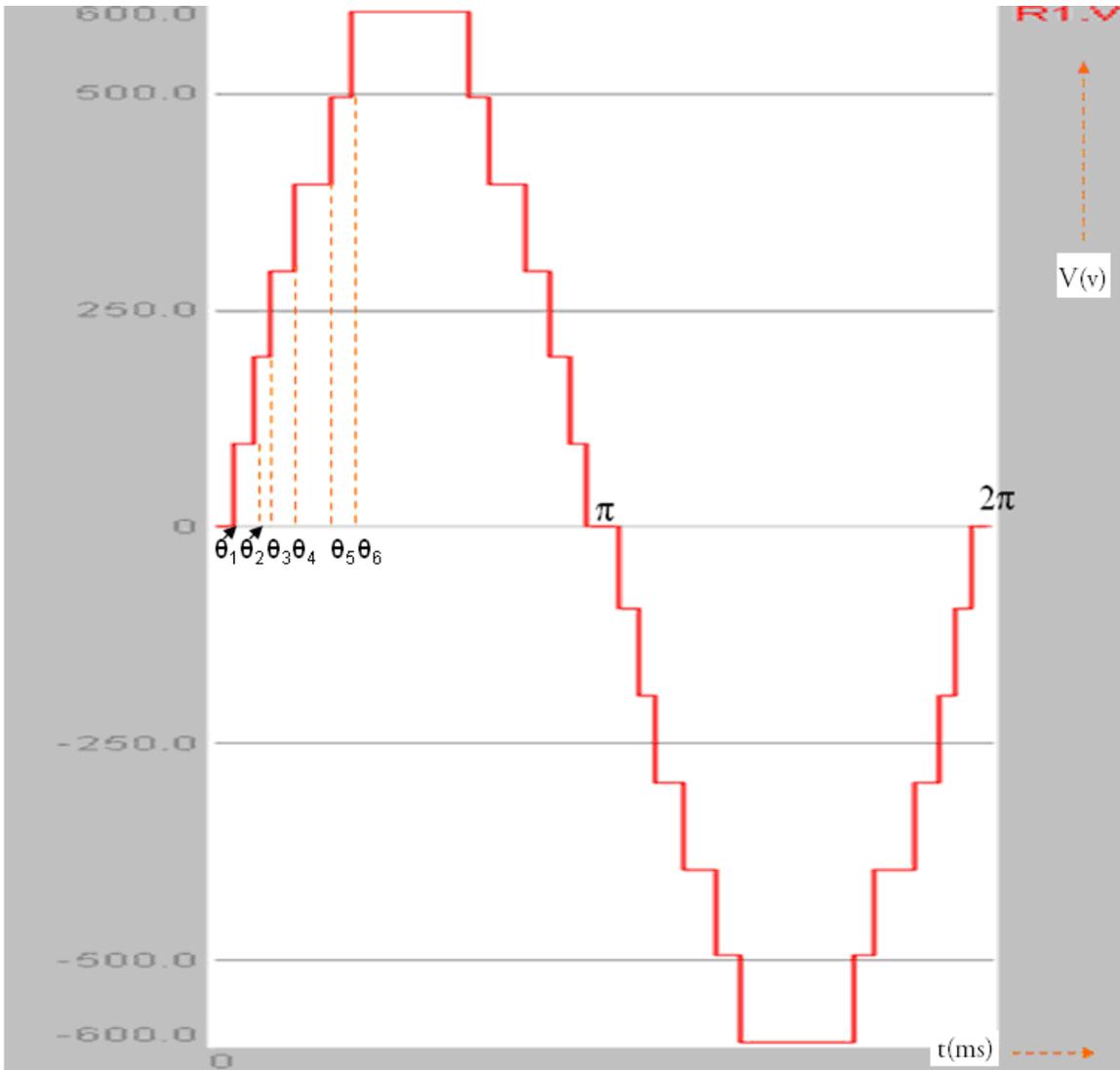
**Figure 16:** Produced voltage employing the modified switching scheme

The switching table for the synthesis of the staircase voltage is listed in Table V.

**Table V:** Switching table

Voltage in Volts	BJT 1	BJT 2	BJT 3	BJT 4	BJT 5	BJT 6	BJT 7	BJT 8	BJT 9	BJT 10	BJT 11	BJT 12
600	1	0	0	1	1	0	0	1	1	0	0	1
500	1	0	0	1	1	0	0	1	1	0	1	0
400	1	0	0	1	1	0	1	0	1	0	0	1
300	1	0	1	0	1	0	0	1	1	0	0	1
200	1	0	1	0	1	0	0	1	1	0	1	0
100	1	0	1	0	1	0	1	0	1	0	0	1
0	1	0	1	0	1	0	1	0	1	0	1	0
-100	0	1	0	1	0	1	0	1	0	1	1	0
-200	0	1	0	1	0	1	1	0	0	1	0	1
-300	0	1	0	1	0	1	1	0	0	1	1	0
-400	0	1	1	0	0	1	0	1	0	1	1	0
-500	0	1	1	0	0	1	1	0	0	1	0	1
-600	0	1	1	0	0	1	1	0	0	1	1	0

The output voltage from the converter is a seven-level staircase voltage and is shown in Figure 17.



**Figure 17:** Seven level staircase voltage

Applying Fourier analysis on the above waveform, we get the following equation.

$$v(t) = \frac{4}{\pi} \sum_k \left( \begin{array}{l} V_1 \cos(k\theta_1) + V_2 \cos(k\theta_2) + V_3 \cos(k\theta_3) + \\ (V_1 + V_3) \cos(k\theta_4) + (V_2 + V_3) \cos(k\theta_5) + \\ (V_1 + V_2 + V_3) \cos(k\theta_6) \end{array} \right) \sin(k\omega t) \quad (25)$$

$k = 1, 3, 5 \dots \infty$

$$V_1 = E_3 = V_{dc}$$

$$V_2 = E_2 = 2V_{dc}$$

$$V_3 = E_1 = 3V_{dc} \quad (26)$$

$$V_{dc} = 100V$$

The modified switching scheme thus produces a 100 V step with every rise and fall in the staircase voltage. The transcendental equation is given as follows.

$$\frac{4.V_{dc}}{\pi} [\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4) + \cos(\theta_5) + \cos(\theta_6)] = V_1$$

$$[\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4) + \cos(5\theta_5) + \cos(5\theta_6)] = 0$$

$$[\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4) + \cos(7\theta_5) + \cos(7\theta_6)] = 0$$

$$[\cos(11\theta_1) + \cos(11\theta_2) + \cos(11\theta_3) + \cos(11\theta_4) + \cos(11\theta_5) + \cos(11\theta_6)] = 0$$

$$[\cos(13\theta_1) + \cos(13\theta_2) + \cos(13\theta_3) + \cos(13\theta_4) + \cos(13\theta_5) + \cos(13\theta_6)] = 0$$

$$[\cos(17\theta_1) + \cos(17\theta_2) + \cos(17\theta_3) + \cos(17\theta_4) + \cos(17\theta_5) + \cos(17\theta_6)] = 0$$

(27)

The value of  $V_1$  was assumed as 600 V. Solving (27) we get a set of values for the firing angles which will eliminate  $(m-2)$  odd harmonics from the system. In this system, we consider the elimination of the fifth, seventh, eleventh, thirteenth and the seventeenth harmonics from the system. The triplen harmonics are not solved under the assumption that the triplens cancel out each other in a balanced three phase network, as discussed earlier.

The above transcendental equations were solved using MAPLE<sup>®</sup> software. The transcendental equations were solved using the *fsolve* command in the software. The resulting angles in radians were converted into degrees and are listed as follows.

$$\begin{aligned}\theta_1 &= 7.86^\circ, \theta_2 = 16.625^\circ, \theta_3 = 24.5^\circ, \\ \theta_4 &= 36.628^\circ, \theta_5 = 53.253^\circ, \theta_6 = 63.185^\circ\end{aligned}\tag{28}$$

The angles computed above do not result in absolute zero magnitudes of the odd harmonics intended to be completely eliminated, although they are relatively small compared to the fundamental component. They are listed below.

$$\begin{aligned}\hat{V}_1 &= 599.78 V, \hat{V}_5 = 1.4 V, \hat{V}_7 = 1.8 V, \hat{V}_{11} = -0.52 V, \\ \hat{V}_{13} &= -0.94 V, \hat{V}_{17} = -0.08 V\end{aligned}$$

The non-zero and negative amplitudes of the harmonics are due to the limits of computational precision. As a result of processor clock speed, the hardware implementation will face similar limitations while programming the angles.

### 3.2 Voltage sensitivity analysis

Harmonic elimination discussed in section 2.3, shows that the harmonics depends on the magnitudes of the DC voltage sources and the firing angles obtained by solving the transcendental equations. The firing angles are pre-calculated and are preprogrammed in the firing control device (e.g. a microprocessor). Voltage sensitivity analysis is performed to measure the impact of change in voltage magnitude of the DC sources on

harmonic elimination. Rewriting the transcendental equations of the output voltage from equation (25),

$$v(t) = \frac{4}{\pi} \sum_k \left( \begin{array}{l} E_3 \cos(k\theta_1) + E_2 \cos(k\theta_2) + E_1 \cos(k\theta_3) + \\ (E_1 + E_3) \cos(k\theta_4) + (E_2 + E_1) \cos(k\theta_5) + \\ (E_3 + E_2 + E_1) \cos(k\theta_6) \end{array} \right) \sin(k\omega t)$$

$$k = 1, 3, 5 \dots \infty$$

$$E_1 = 300 \text{ V}, E_2 = 200 \text{ V and } E_3 = 100 \text{ V}.$$

Consider a change in the magnitude of source  $E_2$ . The impact of the change in magnitude of the source in the change in the peak values of the higher order harmonics is analyzed as follows.

The Fourier equation for the magnitude of higher order harmonic is as follows.

$$\hat{V}_k = \frac{4}{\pi} \left( \begin{array}{l} E_3 \cos(k\theta_1) + E_2 \cos(k\theta_2) + E_1 \cos(k\theta_3) + \\ (E_1 + E_3) \cos(k\theta_4) + (E_2 + E_1) \cos(k\theta_5) + \\ (E_3 + E_2 + E_1) \cos(k\theta_6) \end{array} \right) \quad (29)$$

$$k = 1, 5, 7, 11, 13, 17$$

The voltage sensitivity is obtained by the partial differentiation of the above equation with respect to the voltage. Partial differentiation of equation 29 with respect to  $E_2$  yields,

$$\frac{\partial \hat{V}_k}{\partial E_2} = \frac{4}{\pi} [\cos(k\theta_2) + \cos(k\theta_5) + \cos(k\theta_6)] \quad (30)$$

The initial values of the firing angles have been computed and are listed in equation (28).

Evaluating the above equation at the initial values of theta,

$$\left. \frac{\partial \hat{V}_k}{\partial E_2} \right|_{\theta_i = \theta_i^0} = \frac{4}{\pi} [\cos(16.625 \times k) + \cos(53.253 \times k) + \cos(63.185 \times k)] \quad (31)$$

$$\left. \frac{\partial \hat{V}_1}{\partial E_2} \right|_{\theta_i = \theta_i^0} = 2.56,$$

$$\left. \frac{\partial \hat{V}_5}{\partial E_2} \right|_{\theta_i = \theta_i^0} = 0.98,$$

$$\left. \frac{\partial \hat{V}_7}{\partial E_2} \right|_{\theta_i = \theta_i^0} = 0.80,$$

$$\left. \frac{\partial \hat{V}_{11}}{\partial E_2} \right|_{\theta_i = \theta_i^0} = -1.05,$$

$$\left. \frac{\partial \hat{V}_{13}}{\partial E_2} \right|_{\theta_i = \theta_i^0} = -0.15,$$

$$\left. \frac{\partial \hat{V}_{17}}{\partial E_2} \right|_{\theta_i = \theta_i^0} = 0.275$$

Similarly, the impact of change in the voltage magnitudes of the other sources are evaluated and listed in Table VI.

**Table VI: Sensitivity table**

DC source	Sensitivity equation	Harmonic					
		1 <sup>st</sup>	5 <sup>th</sup>	7 <sup>th</sup>	11 <sup>th</sup>	13 <sup>th</sup>	17 <sup>th</sup>
E <sub>3</sub>	$\frac{\partial \hat{V}_k}{\partial E_3} = \frac{4}{\pi} \begin{bmatrix} \cos(k\theta_1) \\ + \cos(k\theta_4) \\ + \cos(k\theta_6) \end{bmatrix}$	2.86	0.48	-0.5	0.05	0.01	2.11
E <sub>2</sub>	$\frac{\partial \hat{V}_k}{\partial E_2} = \frac{4}{\pi} \begin{bmatrix} \cos(k\theta_2) \\ + \cos(k\theta_5) \\ + \cos(k\theta_6) \end{bmatrix}$	2.56	0.98	0.80	-1.005	-0.15	0.275
E <sub>1</sub>	$\frac{\partial \hat{V}_k}{\partial E_1} = \frac{4}{\pi} \begin{bmatrix} \cos(k\theta_3) \\ + \cos(k\theta_4) \\ + \cos(k\theta_5) \\ + \cos(k\theta_6) \end{bmatrix}$	3.52	-1.12	-0.15	1.19	1.26	0.54

Table VI gives us the information on the impact of variations in the DC source magnitude on harmonic elimination. The higher the value of the sensitivity number in the switching table, the more is the sensitivity of that particular harmonic.. The first harmonic is the most sensitive to the DC source voltage variations. The information will help us understand the impact of voltage variations and develop suitable controls to offset the effects of DC source voltage variations in harmonic elimination and to maintain a magnitude of the fundamental wave as a constant.

The voltage sensitivity for a classical cascaded multilevel converter is as follows. The transcendental equation for the classical cascaded multilevel converter is given in equation.

$$\hat{V}_k = \frac{4}{\pi} (E_3 \cos(k\theta_1) + (E_2 + E_3) \cos(k\theta_2) + (E_1 + E_2 + E_3) \cos(k\theta_3)) \quad (32)$$

$$k = 1, 5, 7, 11, 13, 17$$

For a voltage magnitude variation in one of the sources (e.g.  $E_2$ ), the sensitivity equation is obtained by partial differentiation of equation 32.

$$\frac{\partial \hat{V}_k}{\partial E_2} = \frac{4}{\pi} [\cos(k\theta_2) + \cos(k\theta_3)]$$

The values of thetas for the classical cascaded multilevel converter were computed and the sensitivities at the initial values of thetas were evaluated.

$$\theta_1 = 11.682^\circ, \theta_2 = 31.182^\circ, \theta_3 = 58.579^\circ$$

$$\left. \frac{\partial \hat{V}_1}{\partial E_2} \right|_{\theta_i = \theta_i^0} = 1.75,$$

$$\left. \frac{\partial \hat{V}_5}{\partial E_2} \right|_{\theta_i = \theta_i^0} = 0,$$

$$\left. \frac{\partial \hat{V}_7}{\partial E_2} \right|_{\theta_i = \theta_i^0} = 0,$$

$$\left. \frac{\partial \hat{V}_{11}}{\partial E_2} \right|_{\theta_i = \theta_i^0} = 1.38,$$

$$\left. \frac{\partial \hat{V}_{13}}{\partial E_2} \right|_{\theta_i = \theta_i^0} = 0.72,$$

$$\left. \frac{\partial \hat{V}_{17}}{\partial E_2} \right|_{\theta_i = \theta_i^0} = -2.33$$

The sensitivity of the classical cascaded multilevel converter is listed in Table

VII.

**Table VII:** Sensitivity table (classical cascaded MLC)

DC source	Sensitivity equation	Harmonic					
		1 <sup>st</sup>	5 <sup>th</sup>	7 <sup>th</sup>	11 <sup>th</sup>	13 <sup>th</sup>	17 <sup>th</sup>
E <sub>3</sub>	$\frac{\partial \hat{V}_k}{\partial E_3} = \frac{4}{\pi} \begin{bmatrix} \cos(k\theta_1) \\ + \cos(k\theta_2) \\ + \cos(k\theta_3) \end{bmatrix}$	3	0	0	1.38	0.72	-2.33
E <sub>2</sub>	$\frac{\partial \hat{V}_k}{\partial E_2} = \frac{4}{\pi} \begin{bmatrix} \cos(k\theta_2) \\ + \cos(k\theta_3) \end{bmatrix}$	1.75	-0.66	-0.18	1.53	1.85	-1.12
E <sub>1</sub>	$\frac{\partial \hat{V}_k}{\partial E_1} = \frac{4}{\pi} [\cos(k\theta_3)]$	0.66	0.49	0.82	0.32	0.95	0.13

From the two sensitivity tables, it can be concluded that the proposed scheme is more sensitivity to dc source magnitude variations for the first three harmonics i.e. 1<sup>st</sup>, 5<sup>th</sup>

and 7<sup>th</sup>. The higher order harmonics in the classical scheme, which are not even eliminated, are more sensitive to the dc source magnitude variations which should have a larger impact in the THD.

The negative values of some of the sensitivities are nonsensical, given that the amplitudes (always positive numbers) are ideally zero when eliminated. However, as discussed earlier, the computational precision of the angles did not yield these ideal values but some negative ones too. This could be interpreted as the introduction of phase shifts for these harmonics due to this lack of precision, and a negative sensitivity would indicate a further reduction of the amplitude from a negative value.

For example, for a one volt change in the magnitude of source E2, the magnitude of the 11<sup>th</sup> harmonic (sensitivity = -1.05) changes from -0.5 V to -1.52 V.

### **3.3 Source and switch utilization**

Source utilization is the time period over which an electric source is employed. It is the time period a source conducts in a cycle. Source utilization provides us the information on the discharge rates of the DC sources employed in the cascaded multilevel converter. The source utilization has to be equal or as close as possible. The firing angles computed from the transcendental equations provide us the information on the turn on and turn off of the sources for harmonic elimination. The firing angles are listed in equation 28, and the source utilization is computed.

The source utilization for a 100 ohm load is as follows. During the second step of the staircase, the 100 volt source is turned ON which supplies 1 A of current for 0.41443 ms. The current put by the sources are the same as they are connected in series. The ampere hours of each source is the product of current supplied by the source at each step of the staircase and its respective time. The current supplied by each source and their respective times over half a period are listed in Table VIII.

**Table VIII:** Source utilization

<b>Current</b>	<b>E1</b>	<b>E2</b>	<b>E3</b>
1	0	0	0.41443
2	0	0.35643	0
3	0	0.56197	0.56197
4	0.76977	0	0.76977
5	0.46004	0.46004	0
6	2.4829	2.4829	2.4829

Source utilization of source E3 is computed as an example.

$$U_{E3} = 2 \times (0.41443 \times 1) + (0.56197 \times 3) + (0.76977 \times 4) + (2.4829 \times 6)$$

$$U_{E3} = 40.15364 \text{ Ams}$$

The source utilization is 36.78182 Ams for 100 V source, 39.19274 Ams for the 200 V source and 40.55336 Ams for the 300 V source. The source utilizations are not identical as in the classical cascaded multilevel converter, which has equal source utilization. However, the source utilizations in the proposed cascaded multilevel converter are not that far apart and can be employed in photovoltaic applications where the dc source is continuously charged by photovoltaic arrays during the day time.

Switch utilization is defined as the time period a switch conducts in one cycle. Semiconductor switches are turned on and off as per the desired switching pattern. The switch utilization is calculated to compute the conduction time of each switch. The conduction time of the switches need to be equal or as close as possible. This is to ensure that the wear and tear of the switches is equal, which will help in maintenance and replacement. The switch utilization is computed with the information listed in equation 28. The switch utilization is 8.33 ms for all the switches for a 60 Hz cycle.

With the above information, analysis is performed to obtain an equal switch and source utilization.

## **CHAPTER IV**

### **SIMULATION**

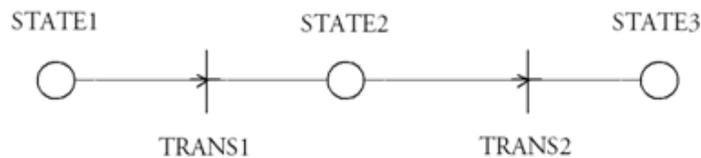
The simulation of the cascaded MLC was performed using Ansoft's Simplorer<sup>®</sup> software. The circuit was built in the software from the devices available in the software's model library. The commutation of the transistor switches in the cascaded MLC was controlled with state machines. The 5<sup>th</sup>, 7<sup>th</sup>, 11<sup>th</sup>, 13<sup>th</sup> and the 17<sup>th</sup> harmonics were expected to be eliminated by applying harmonic elimination technique. Fourier analysis was obtained from the simulated waveform to verify the theory. The simulation also yielded THD of the resultant waveform. The simulation was first carried out for a single-phase inverter and then for a three phase wye-delta connected inverter. The frequency spectrum and the THD for both cases were verified. This section explains the model development, state machine programming and the analysis of the simulated output waveform.

## 4.1 State machine programming

A state machine is a circuit with internal states [14]. A state specifies a unique internal condition of a system. There are two types of state machines.

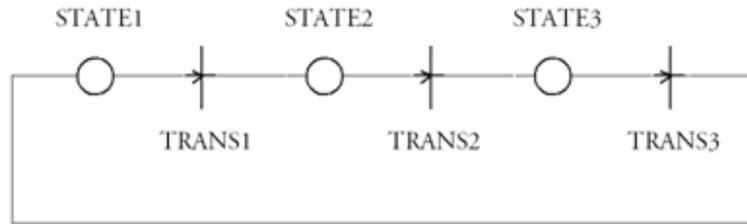
- i. Open loop state machine and
- ii. Closed loop state machine

An open loop state machine begins with an active state and stops at the end of the last state. An open loop state machine can be used for a non-repetitive event. An open loop state machine is shown in Figure 18.



**Figure 18:** Open loop state machine

A closed loop state machine begins with an active state and at the execution of the last state, it loops back to the first state or the active state. The closed loop state machine can be employed for a repetitive event. A closed loop state machine is shown in Figure 19.

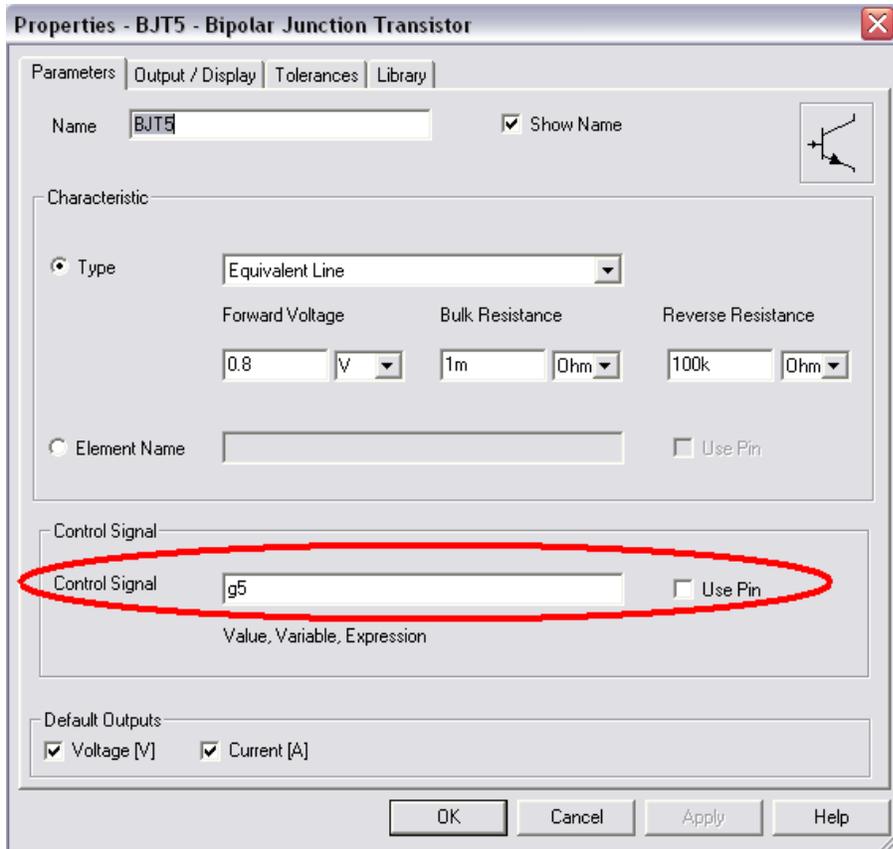


**Figure 19:** Closed loop state machine

In Simplorer<sup>®</sup> the state machine is based on Petri Net theory [15]. The state machine allows us to model and control event driven processes. The model allows the user to control and run event driven simulations. In the state machines shown in Figure 18 and Figure 19, the states are the events. The transition (*trans*) identifies the condition for transfer from one event to the next.

The cascaded MLC is controlled by the gate pulses to the transistors. The gate pulses to the converter are provided by programming a state machine. In order to control the transistor using a control variable, the device property has to be modified. Double clicking on the device opens the device property window.

The control signal of the device is listed under the parameters tab of the property window. The property window of BJT5 is shown in Figure 20. The use of the pin option is unchecked and the name of the control variable is entered as shown in Figure 20. Thus the control signal for each of the transistors present in the model is set.

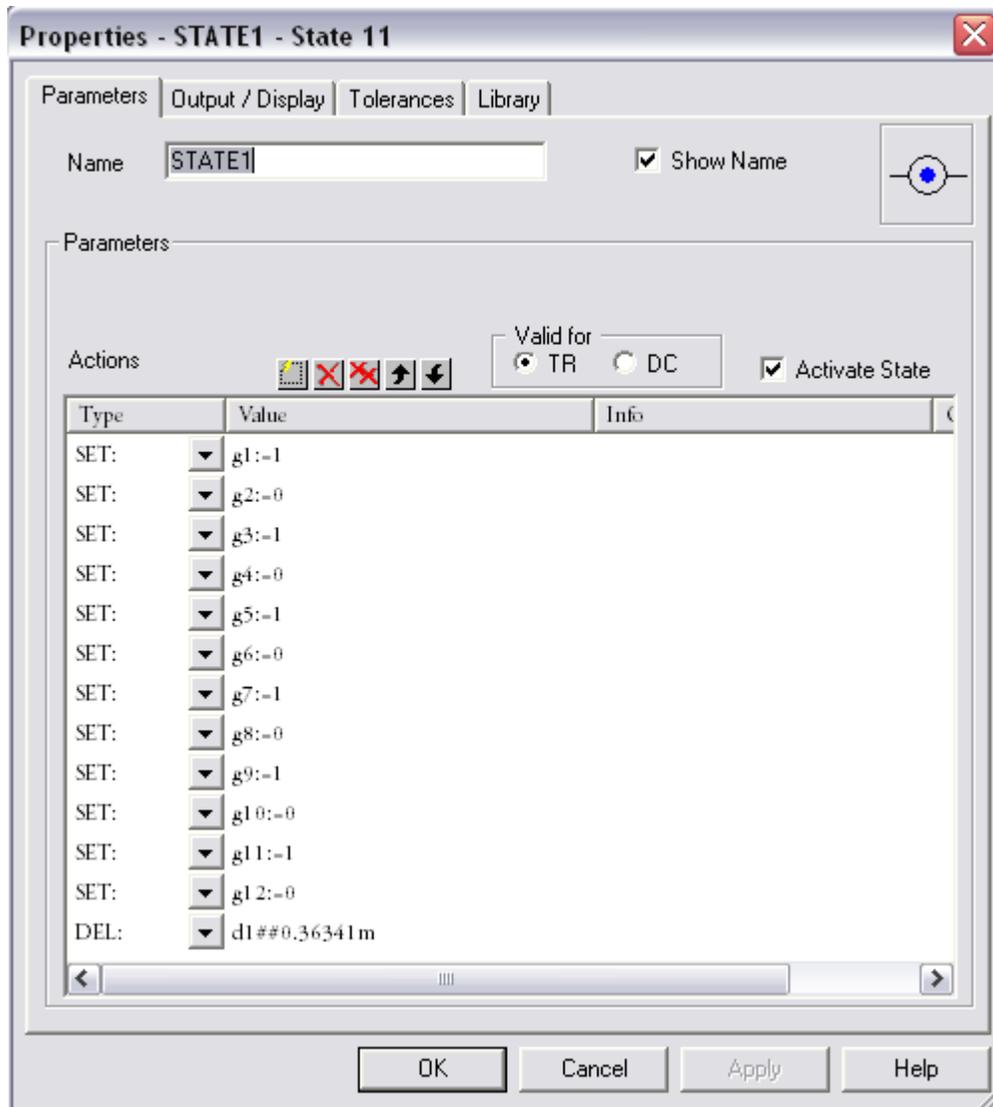


**Figure 20:** Device property window

Double clicking on the state in the state machine opens up the state property window. The program of every state is entered in this window. The status of all the transistors in the model can be specified in the state program using the *SET* command. The *SET* command sets the value of a gate control variable. The syntax for the *SET* command is

*SET "variable name: = 0/1".*

For example, *SET g5:=1* will turn on the transistor and *SET g5:=0* will turn the transistor off. The window for a state in the state machine is shown in Figure 21.



**Figure 21:** State program window

The state machine controls all the switches in the simulation. The status of all the switches has to be mentioned in each state. The variables g1 to g12 controls the switching of the respective switch in the cascaded multilevel converter.

The time for transition in the state machine from one state to the next is determined by the value of firing angles previously calculated. It is converted in to time in seconds using equation

$$t_n = \frac{(\theta_{n+1} - \theta_n) \times 8.3333}{180} \quad (32)$$

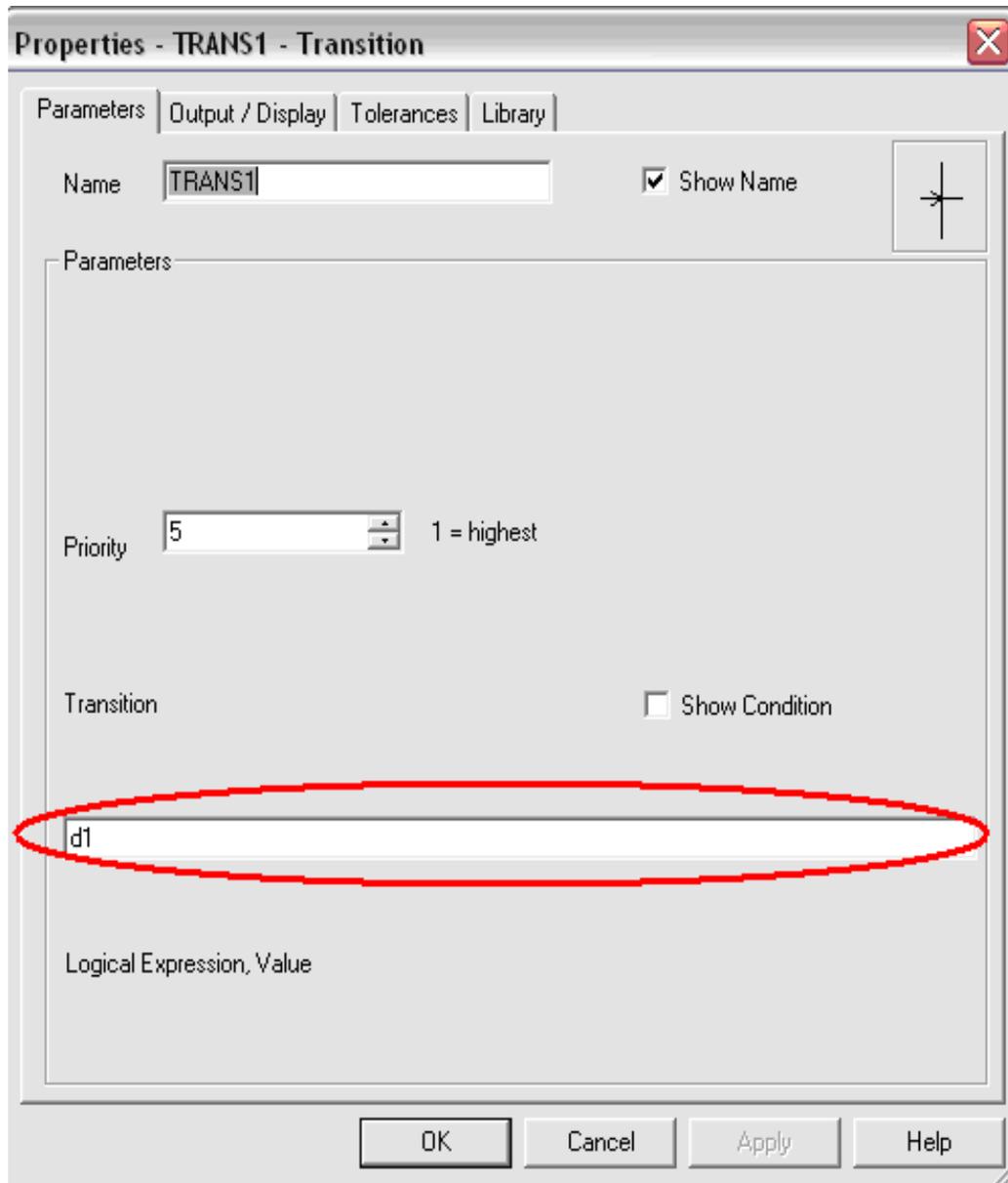
In equation 33, the value 8.33 corresponds to the half cycle time period of a 60 Hz system and 180 is the cycle period in degrees.

The *DEL* command delays the validation of a variable from false condition to the true condition for the time mentioned in its syntax (to the right of the ## symbol). The syntax for *DEL* command is

*DEL* “variable name ## time”

For example, ‘*DEL d1 ## 0.1 m*’ will delay the validation of the variable *d1* from low to high state for one millisecond. The *DEL* command works in conjunction with the transition in the state machine.

The condition for transition from one state to next state is specified in the transition and the condition is controlled in the state program. For example, the *DEL* command delays the validation of the variable *d1* by one millisecond. When the variable *d1* is validated from a false condition to true condition at the end of one millisecond, the transition identifies the validation and moves from the current state to the next state. The variable for state transition has to be specified in the transition. Double clicking on the transition opens the transition property window, where the transition variable is specified. A transition property window is shown in Figure 22. In the window, the priority value is not changed as we are not prioritizing any state transitions and is set at the default value unaltered.

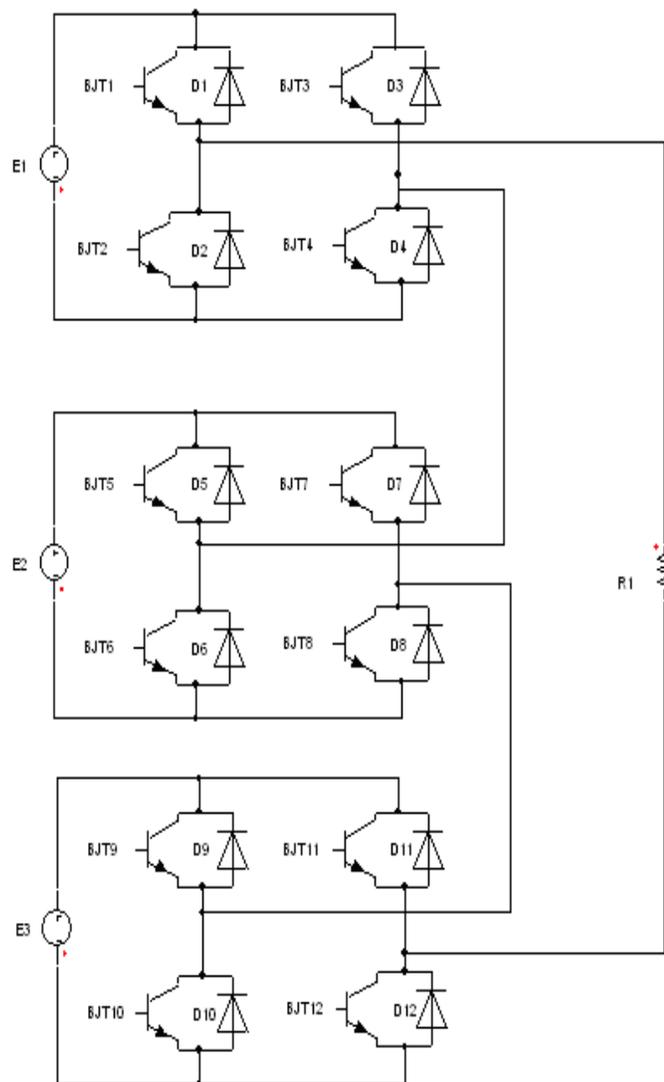


**Figure 22:** Transition property window

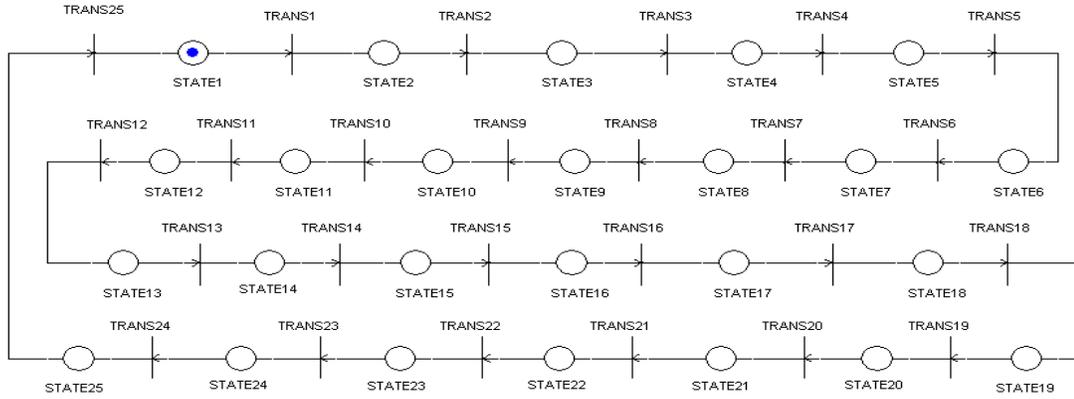
Thus a state machine is constructed for the proposed cascaded MLC. Each voltage step in the staircase waveform of the cascaded MLC requires a state. Single-phase and three-phase cascaded MLC were designed and controlled using state machines.

## 4.2 Single-phase cascaded MLC

The model of a cascaded MLC developed using the software is shown in Figure 23. The magnitudes of the three voltage sources E1, E2 and E3 in the model are 300 V, 200 V and 100 V respectively. The state machine for the single-phase model is shown in Figure 24.



**Figure 23:** Single-phase cascaded MLC

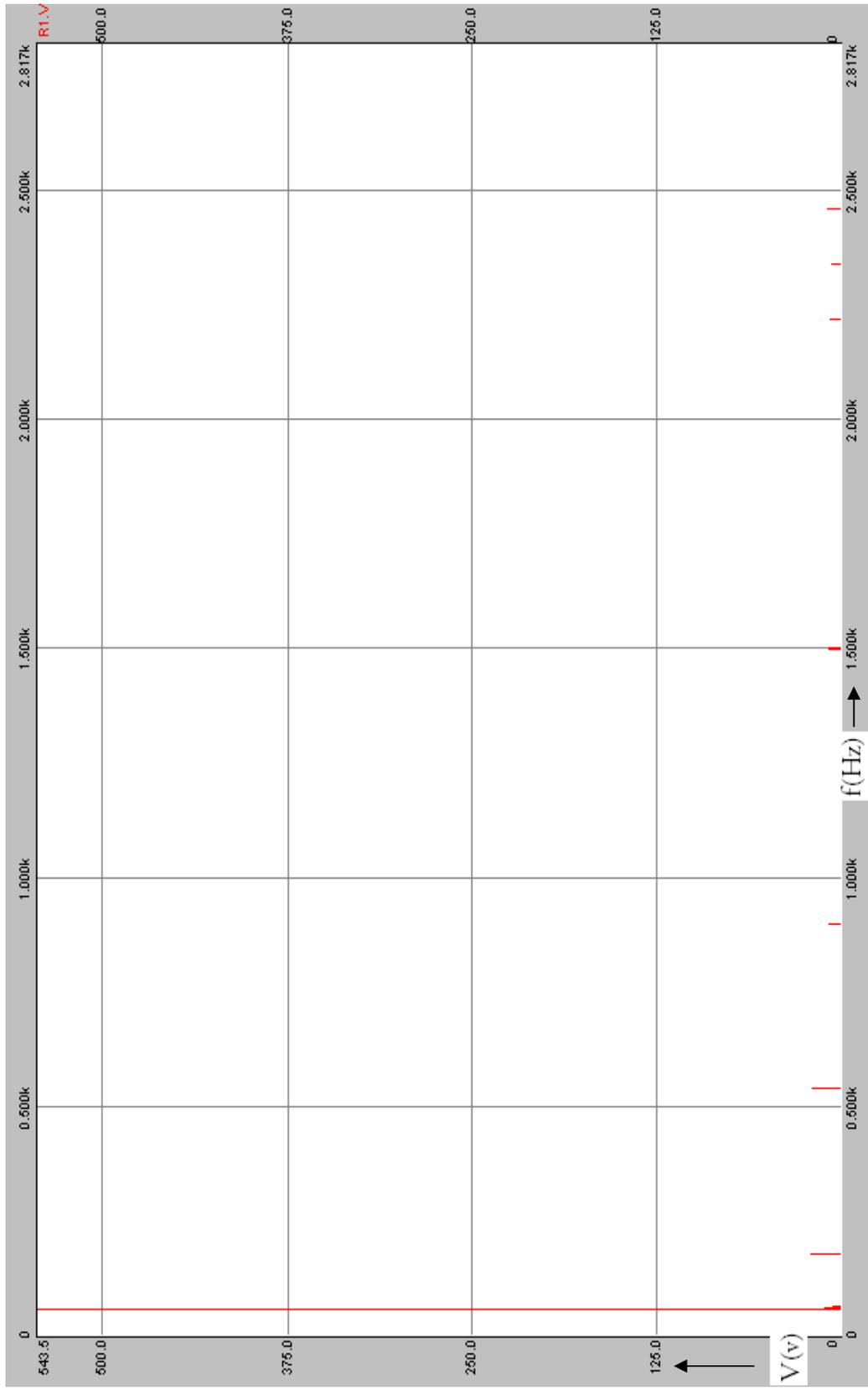


**Figure 24:** State machine for single-phase cascaded MLC

The active state in the state machine is marked with a dot at its center as shown in Figure 24. After the completion of one cycle, the state restarts from the first active state once more and it continues till the end of the specified simulation time. The simulated single-phase seven-level voltage waveform is shown in Figure 25.

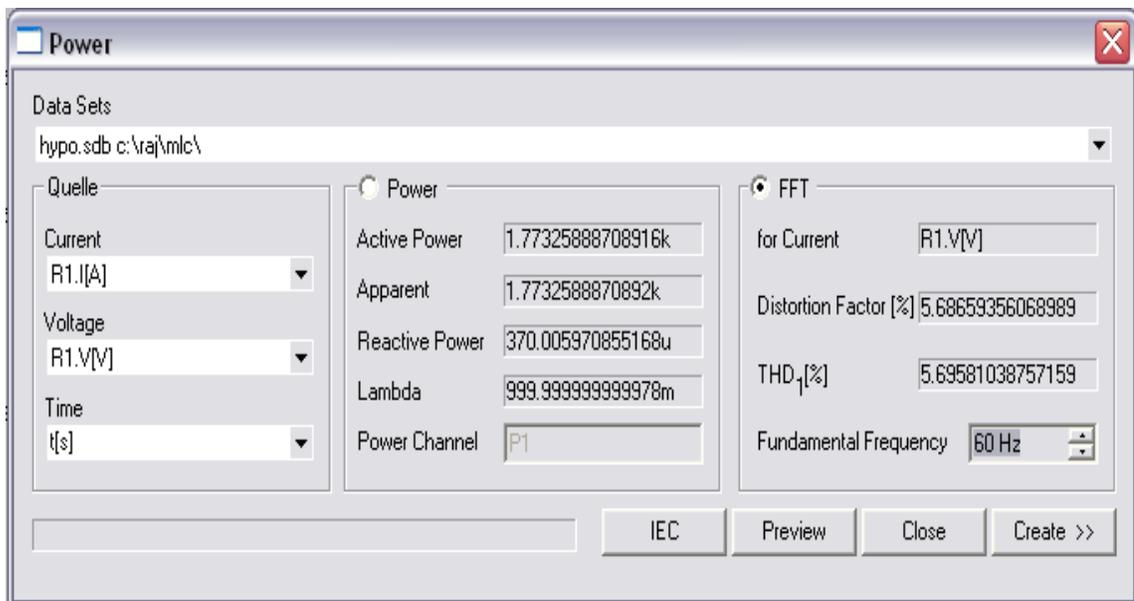


The Fourier analysis and the evaluation of the THD in the simulated waveform was performed using the 'day-post-processor' tool. The frequency spectrum of the simulated single-phase waveform is shown in Figure 26.



**Figure 26:** Frequency spectrum of the single-phase voltage

The frequency spectrum of the simulated voltage shows that the intended odd harmonics, i.e. the fifth, the seventh, the eleventh, the thirteenth and the seventeenth harmonics are indeed eliminated from the system. The triplen harmonics are still present in the output voltage which is undesirable and does not meet the standards. The THD in the voltage is computed using the day post processor. The THD of the produced voltage was found to be 5.69 % and is above the standard limitations of 5 %. The power window which displays the THD is shown in Figure 27.



**Figure 27:** Power window with THD

The simulation was also performed on an inductive and capacitive load. The frequency spectrum and the THD of the simulation were obtained. The frequency spectrum of the simulation with an inductive load is shown in Figure 28. The THD is shown in Figure 29. The frequency spectrum shows that the proposed harmonics are eliminated from the system. The THD of the inductive system is 1.69 % which is lesser than the resistive load.



**Figure 28:** Frequency spectrum for an inductive load

**Power**

Data Sets  
single-phase-cmlc.sdb c:\raj\mlc\

Quelle

Current  
L1.I[A]

Voltage  
L1.V[V]

Time  
t[s]

Power

Active Power 2.3799639312739k

Apparent 455.956400937094k

Reactive Power 455.950189524244k

Lambda 5.21971821512436m

Power Channel P1

FFT

for Current L1.I[A]

Distortion Factor [%] 1.69511749959166

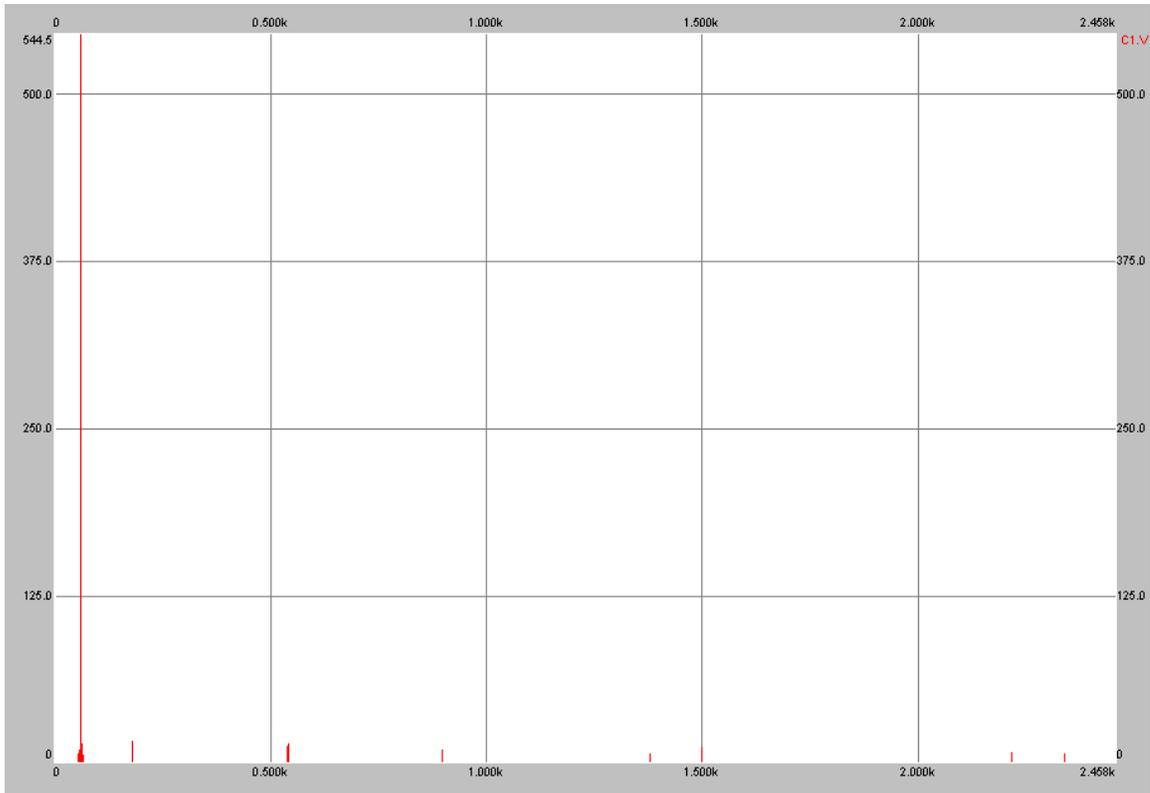
THD<sub>1</sub> [%] 1.69536109159779

Fundamental Frequency 60 Hz

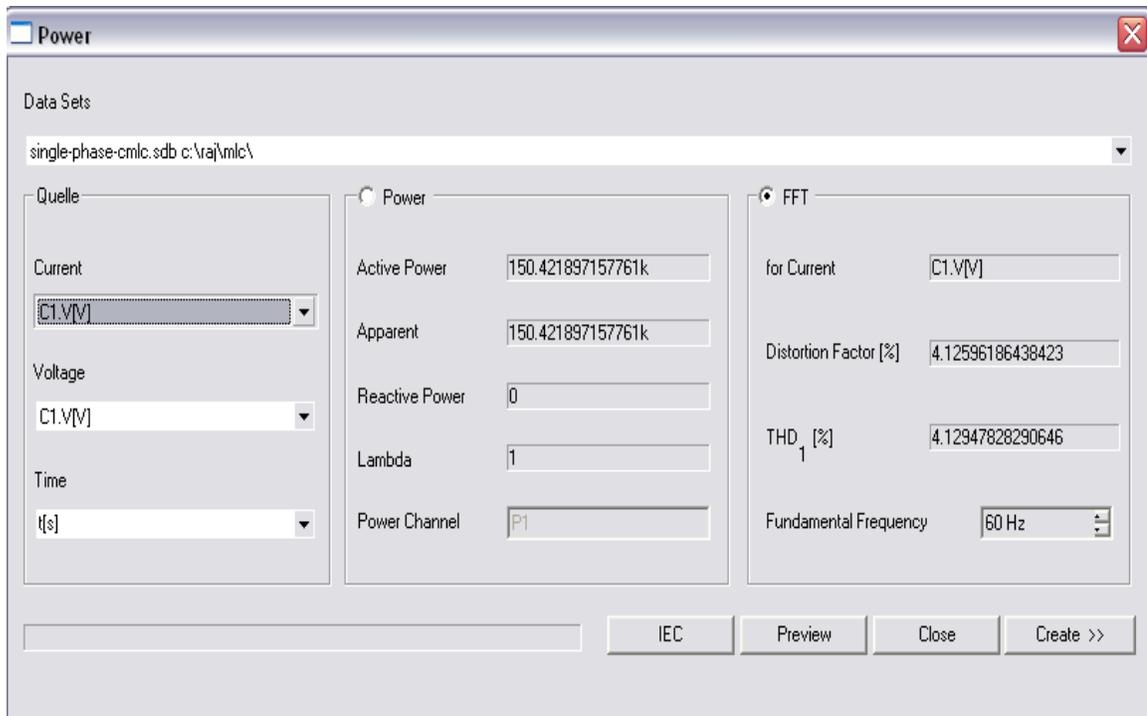
IEC Preview Close Create >>

**Figure 29:** THD of an inductive load

The frequency spectrum of the proposed cascaded MLC with a capacitive load is shown in figure. The THD is shown in figure. The proposed harmonics are eliminated from the system and the THD is 4.13 % and is lesser than the resistive system.



**Figure 30:** Frequency spectrum for a capacitive load



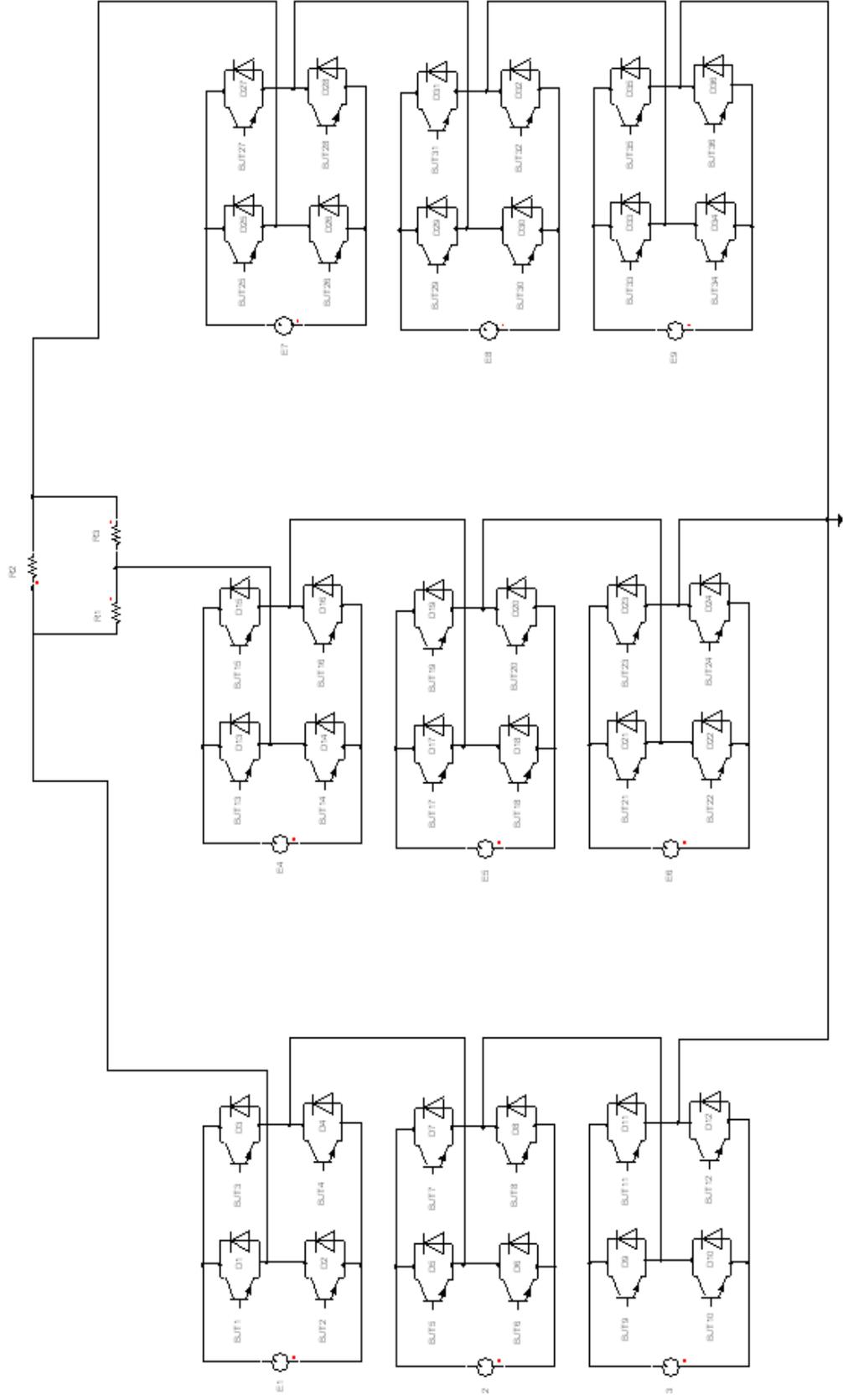
**Figure 31:** THD of a capacitive load

The harmonic elimination technique effectively eliminates the harmonics from the system regardless of the kind of load connected to it. The THD gets better with a capacitive and inductive load.

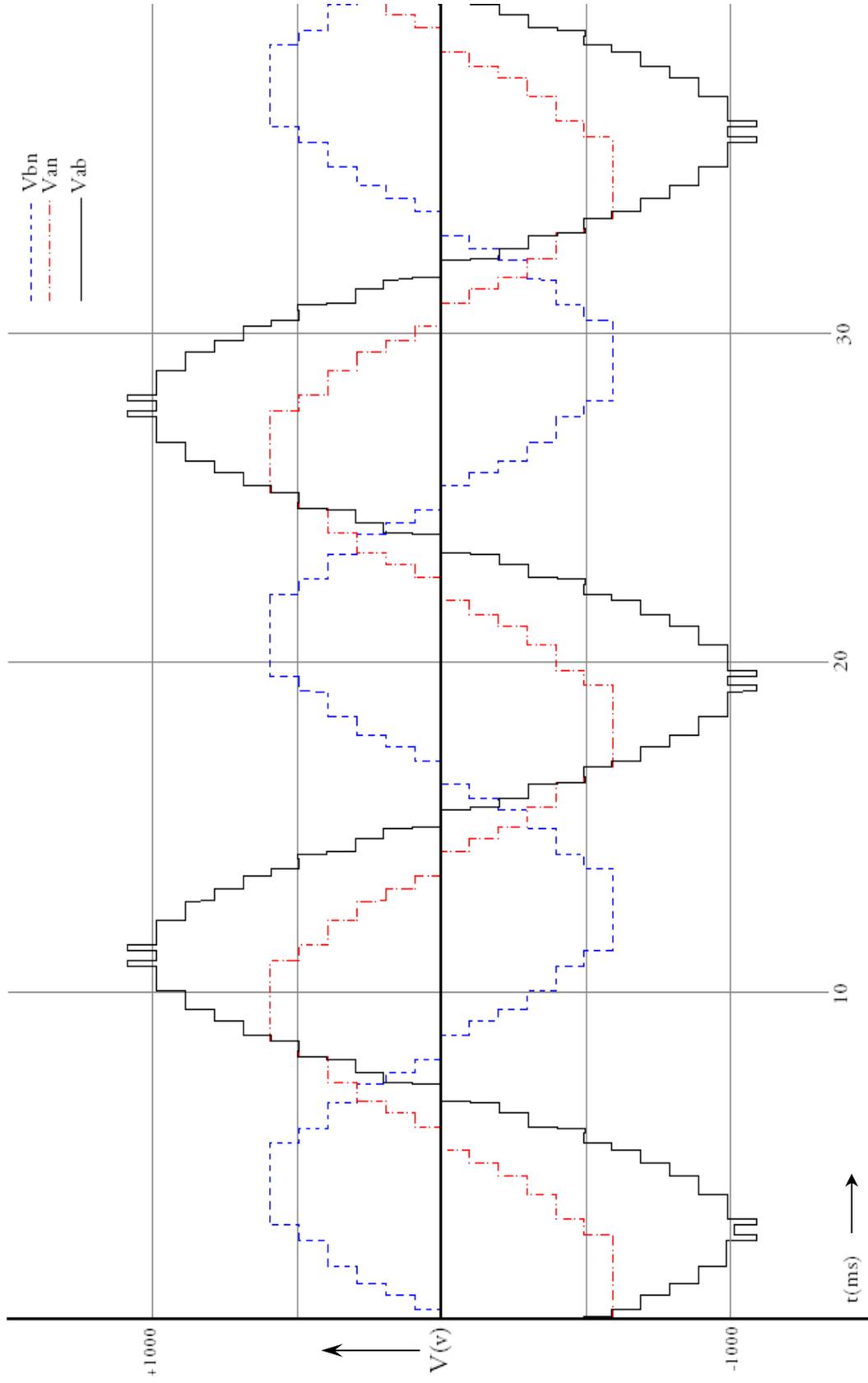
As discussed in section 2.3.1, the triplen harmonics in the output voltage are automatically eliminated. Thus, no attempt was made to cancel them with the switching scheme.

## **4.2 Three-phase cascaded MLC**

In three-phase simulation, three single-phase cascaded MLCs are connected in wye and the load is connected in delta as shown in Figure 32. The model is controlled by three independent state machines. The simulation of the three-phase system was performed the line-to-line voltages were plotted as shown in Figure 33. The line-to-neutral voltage and the resulting line-to-line voltage are tabulated in Table IX.



**Figure 32:** Three-phase MLC circuit diagram

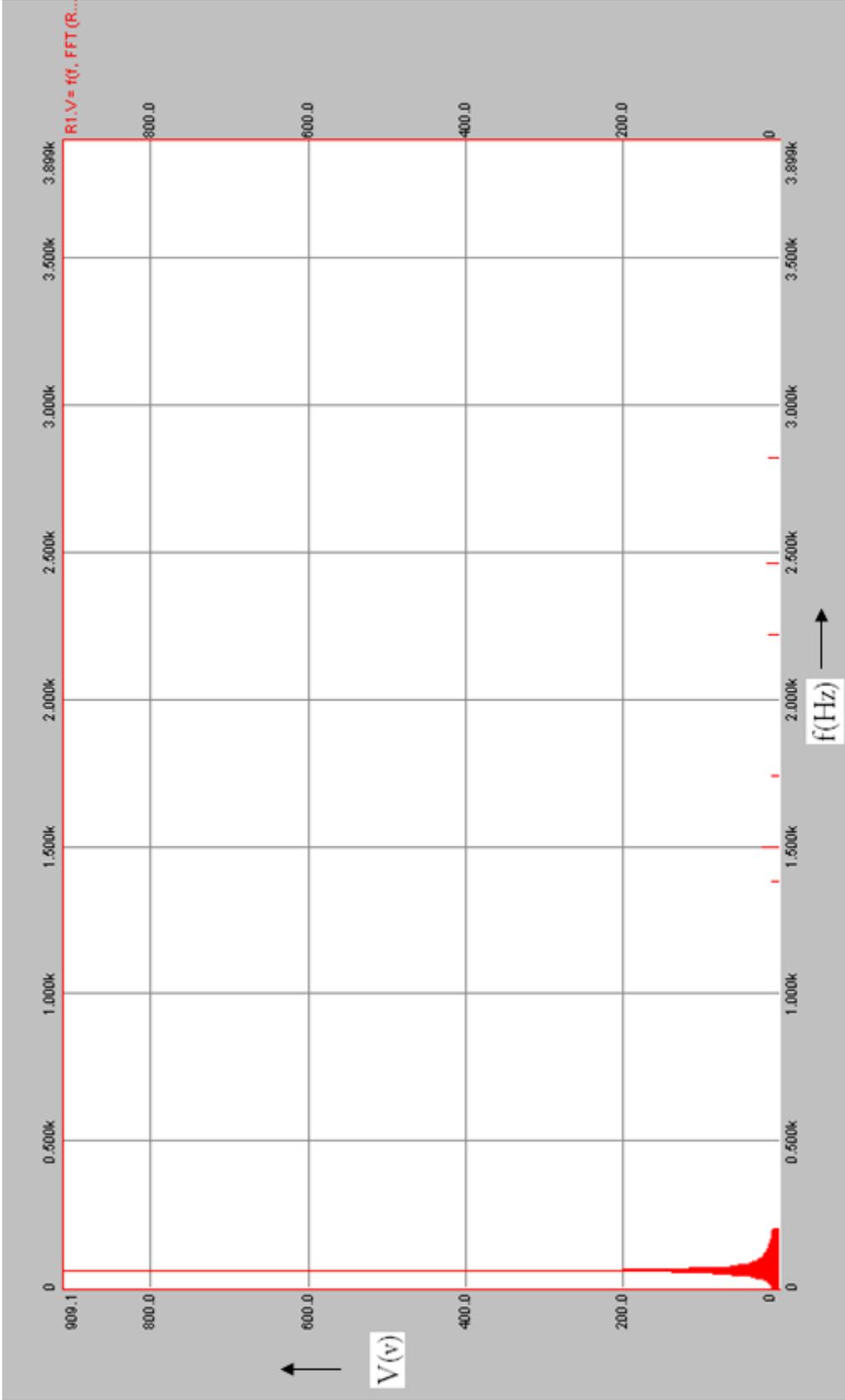


**Figure 33:** Simulated phase and line-to-line voltage

**Table IX:** Line-to-neutral voltage and the resulting line-to-line voltage

$V_{an}$ (V)	$t_{tan}$ (ms)	$\sum t_{tan}$	$V_{bn}$ (V)	$t_{bn}$ (ms)	$\sum t_{bn}$	$V_{ab} (V) = (V_{an} - V_{bn})$	$t_{ab}$ (ms)	$\sum t_{ab}$ (ms)
0	0.36341	0.36341	500	0.14772	0.14772	-500	0.14772	0.14772
-100	0.41443	0.77784				-600	0.21569	0.36341
-200	0.35643	1.13427	600	2.4829	2.63062	-700	0.41443	0.77784
-300	0.56197	1.16924				-800	0.35643	1.13427
-400	0.76977	2.46601				-900	0.56197	1.16924
-500	0.46004	2.92605				-1000	0.76977	2.46601
-600	2.4829	5.40895	500	0.46004	3.09066	-1100	0.16461	2.63062
			400	0.76977	3.86043	-1000	0.29543	2.92605
			300	0.56197	4.4224	-900	0.16461	3.09066
			200	0.35643	4.77883	-800	0.56197	3.86043
			100	0.41443	5.19326	-700	0.41443	4.4224
			0	0.72682	5.92008	-600	0.21569	5.40895
-500	0.46004	5.86899				-500	0.46004	5.86899
-400	0.76977	6.63876	-100	0.41443	6.33451	-400	0.05109	5.92008
-300	0.56197	7.20073	-200	0.35643	6.69094	-300	0.41443	6.33451
						-200	0.30425	6.63876
						-100	0.05218	6.69094
			-300	0.56197	7.25291	0	0.50979	7.20073
-200	0.35643	7.55716				100	0.05218	7.25291
-100	0.41443	7.97159	-400	0.76977	8.02268	200	0.30425	7.55716
0	0.36341	8.335	-500	0.33232	8.335	300	0.41443	7.97159
						400	0.05109	8.02268
						500	0.33232	8.335

As expected, the three-phase configuration cancels out the triplen harmonics from the system and the odd harmonics in the line-to-line voltage of the system. The frequency spectrum of the line-to-line voltage is shown in Figure 34. The frequency spectrum shows that the triplens and the proposed odd harmonics are indeed eliminated from the system. The frequency data is also tabulated in Table X via the simulation software.

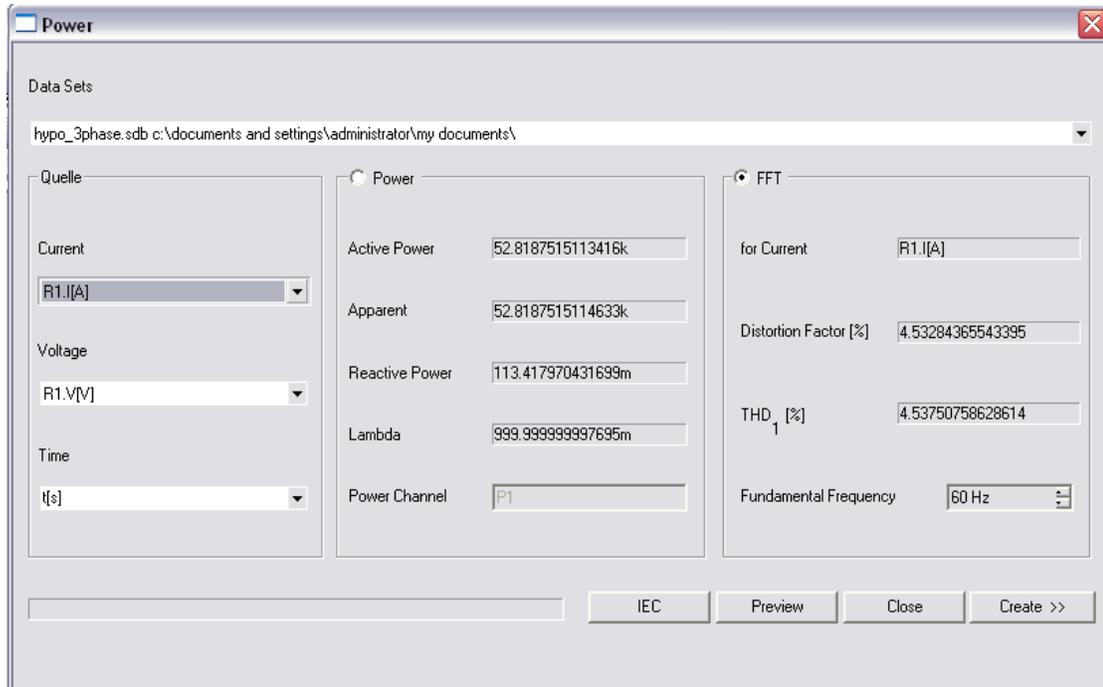


**Figure 34:** Frequency spectrum of the line-to-line voltage

**Table X:** Harmonic table

Harmonic Number	Frequency (Hz)	Amplitude (in Volts)	% Max
1	60	1023.9	100
3	180	0	0
5	300	0	0
7	420	0	0
9	540	0	0
11	660	0	0
13	780	0	0
15	900	0	0
17	1020	0	0
19	1140	0	0
21	1260	0	0
23	1380	12.12	1.18
25	1500	25.62	2.5
27	1620	0	0
29	1740	10.5	1.02
31	1860	13.75	1.34
33	1980	0	0
35	2100	0	0
37	2220	15.95	1.55
39	2340	0	0
41	2460	18.8	1.83
43	2580	0	0
45	2700	0	0
47	2820	12.62	1.23

The power window displaying the THD of the system is shown in Figure 35. It shows that the line to line voltage THD is 4.53%.



**Figure 35:** Power window for three-phase simulation

The salient features of the proposed cascaded multilevel converter are:

- i. More voltage levels from the same number of H-bridges
- ii. More harmonics are eliminated using harmonic elimination
- iii. Lesser THD
- iv. Control of the switches is simpler

## **CHAPTER V**

### **CONCLUSION AND FUTURE WORK**

The topology of the converter is not changed to accommodate the switching scheme for the proposed cascaded MLC. This improves the modularity of the cascaded multilevel converter. Harmonic elimination, which is a salient feature in an MLC, is employed. The following are the improvements in the proposed topology as opposed to the classical cascaded multilevel converter.

In the proposed m-level cascaded MLC, the number of H-bridges required is the same as that of the classical switching scheme. The proposed cascaded multilevel converter produces more voltage levels and the scheme eliminates more harmonics as opposed to the classical cascaded multilevel converter. More harmonics are eliminated from the voltage and the THD as a result is reduced.

The sensitivity analysis data furnishes the details on the sensitivity of the cascaded multilevel converter to changes in the magnitudes of the DC voltage sources. The impact of these DC source voltage variations are quantified to analyze its impact on harmonic elimination and also to maintain the magnitude of the fundamental a constant.

The data can be used to design suitable controls to obtain a constant fundamental and to eliminate the other harmonics from the system.

The simulation results are summarized as follows. In the single-phase cascaded MLC, the THD of the output voltage is 5.69 % and frequency spectrum shows that the triplen harmonics are present. In the three phase simulation, the THD of the output voltage is 4.53 % and the triplens are cancelled out of the system. The source utilization from Table 7 is 40.9 Ah for 100 V source, 71.4 Ah for the 200 V source and 112.9 Ah for the 300 V source. The switch utilization is 8.33 ms for all the switches. Note that the source and switch utilization are calculated over one full cycle. The source and switch utilization were computed manually by adding the time over which the respective switch and source conducts in one full cycle.

## **5.1 Contribution of the thesis**

The results of this work were presented in the 39<sup>th</sup> North American Power Symposium (NAPS 2007) conference [16].

The result of the work was also presented at Ansoft's First Pass system success workshop (2007) [17].

## 5.2 Future work

This work has opened up following potential areas of research.

- i. The prototyping and testing of the proposed cascaded multilevel converter is the primary area of the research.
- ii. The modified switching scheme can be extended to the other two types of multilevel converters, i.e. the diode clamped MLC and the flying capacitor MLC. This will reduce the number of switches in the multilevel converter.
- iii. The back to back operation of cascaded MLCs employing the proposed modification is yet to be analyzed.
- iv. Harmonic elimination technique is limited a few number of voltage steps. This is due to computational complexity involved in solving the transcendental equations. Methods to obtain solutions for the transcendental equations have to be explored.
- v. Based on the voltage sensitivity information suitable control techniques can be implemented to the converter, which will improve the robustness of the converter.
- vi. The sensitivity of the cascaded multilevel converter in harmonic elimination with respect to the firing angles is yet to be analyzed.
- vii. Real time computation of firing angles for harmonic elimination during dynamic voltage variations is yet to be explored. This will help implement

controls to maintain the magnitude of the fundamental voltage constant and eliminate harmonics.

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